

Basavarajeswari Group of Institutions
BALLARI INSTITUTE OF TECHNOLOGY & MANAGEMENT
 (Autonomous Institute under Visvesvaraya Technological University, Belagavi)

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Course Code

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Third Semester B.E. Degree Examinations, September 2024
DIGITAL CIRCUIT DESIGN USING VERILOG

Duration: 3 hrs

Max. Marks: 100

*Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.
 2. Missing data, if any, may be suitably assumed*

<u>Q. No</u>	<u>Question</u>	<u>Marks</u>	<u>(RBTL:CO:PI)</u>
<u>Module-1</u>			
1.	a. A combinational logic circuit which has three inputs, and that produces logic 1 output when even number of variables are at logic 1. Derive the Boolean function	08	(3 :1: 1.7.1)
	b. Define the following (i) Literal (ii) sum term (iii) Minterms (iv) Canonical product of sums (v) SOP (vi) Canonical SOP	06	(2 :1: 1.6.1)
	c. Simplify using K-Map $F(A,B,C,D)=\sum m(0,2,4,9,12,15)+\sum d(1,5,7,10)$	06	(3 :1: 1.7.1)
(OR)			
2.	a. Simplify using 3 variable MEV map. $F(A,B,C,D)=\sum m(3,4,5,7,8,11,12,13,15)$	08	(3 :1: 1.7.1)
	b. Convert the given expression into canonical form $F(A,B,C)=\overline{(C+A)}(\overline{C+B})(A+C)$ $F(A,B,C)=AC+\overline{BC}+AB$	06	(3 :1: 1.7.1)
	c. Explain Multiple Output Function with example.	06	(2 :1: 1.6.1)
<u>Module-2</u>			
3.	a. Explain the importance of HDLs? Explain the two basic digital design methodologies with the help of block diagram.	08	(2 :4:1.6.1)
	b. What is Module? Explain the components of a Verilog module, with the help of block diagram.	06	(2 :4: 1.6.1)
	c. List all the lexical conventions. Explain any 4 lexical conventions with example.	06	(2 :4: 1.6.1)
(OR)			
4.	a. Write the Verilog code for 4 bit ripple carry full adder using gate level modeling	08	(2 :4: 1.7.1)
	b. Define the following data types with examples: Integer, Real, Arrays, Time, memories and parameters.	06	(3 :4: 1.6.1)
	c. Write the Verilog code for Gate-level 4-to-1 multiplexer with stimulus.	06	(3 :4: 1.7.1)

Module-3

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| 5. | a. Define comparator. Design 2 bit comparator. | 08 | (3 :2: 1.6.1) |
| | b. Implement full subtractor using IC74LS138. | 06 | (3 :2:1.7.1) |
| | c. Define Decoder? Design 3:8Active high decoder using logic gates. | 06 | (3 :2: 1.6.1) |

(OR)

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| 6. | a. Explain Full Adder. Realize 4-bit parallel adder and write advantages and disadvantages. | 08 | (3:2: 1.6.1) |
| | b. Implement the following Boolean function using 8:1 multiplexer | 06 | (3 :2: 1.7.1) |

$$F(A, B, C) = \sum m(0, 2, 6, 10, 11, 12, 13) + d(3, 8, 14)$$

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| c. | Define encoder? Explain 4:2 priority encoder. | 06 | (2 :2: 1.6.1) |
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Module-4

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| 7. | a. Define Flip-flop. With a neat circuit and timing diagram explain Negative edge triggered JK Flip-flop | 08 | (2 :3: 1.6.1) |
| | b. Define the flip-flop timing specification : (i)Clock parameters (ii)clock skew (iii)setup (iv)Hold (v)Propagation delay (vi) metastability | 06 | (2 :3: 1.6.1) |
| | c. Define Shift register. With a neat block diagram and truth table explain 4-bit SIPO Register and PISO(Assume the data 1011) | 06 | (2 :3: 1.6.1) |

(OR)

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| 8. | a. A sequential circuit has one input and one output .The state diagram is shown in Fig. Q8 (a). Design a sequential circuit using JK Flip-flops. | 08 | (2 :3: 1.7.1) |
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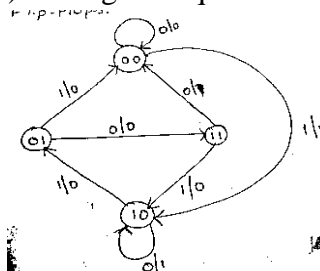


Fig. 8(a)

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| b. | Define Latch. With a neat circuit and timing diagram explain Gated SR Latch | 06 | (2 :3: 1.6.1) |
| | c. Define Asynchronous counter, Explain divide by 8 asynchronous counter | 06 | (2 :3: 1.6.1) |

Module-5

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| 9. | a. What would be the output of the following: a=4'b1100,b=4'b1001
(i) a b (ii) a&b (iii) !a (iv) a<<1 (v) b>>>2 (vi) ~(a^b) (vii) y=a%b (viii) p={{a},2{b}} | 08 | (2 :4: 1.7.1) |
| | b. List the loop statements in Verilog. Explain the following with examples
(i) While loop (ii) For loop (iii) Repeat loop | 06 | (3 :4: 1.6.1) |
| | c. Write a Verilog dataflow description for 4-bit full adder with Carry look ahead | 06 | (3 :4: 1.7.1) |

(OR)

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| 10 | a. Explain the initial and always statement with an example. | 08 | (2 :4: 1.6.1) |
| | b. Explain the blocking assignment statements and non-blocking assignment statements with relevant examples | 06 | (3 :4: 1.6.1) |
| | c. Write a Verilog behavioural description for 4-bit binary counter. | 06 | (3 :4: 1.7.1) |

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