Basavarajeswari Group of Institutions

BALLARI INSTITUTE OF TECHNOLOGY & MANAGEMENT

(Autonomous Institute under Visvesvaraya Technological University, Belagavi)

USN | | | | | | | | | | |

Course Code | 2 | 1 | E | C | 6 | 3 |

Sixth Semester B.E. Degree Examinations – September 2024

FUNDAMENTALS OF VLSI DESIGN

Duration: 3 hrs **Max. Marks: 100**

Note: 1. Answer any* FIVE *full questions choosing ONE full Question from each Module.
2. Missing data, if any, may be suitably assumed

Q. No		*Question*	*Marks*	*(RBTL:CO:PO)*
		Module-1		
1.	**a.**	Explain the following non ideal effects of MOS device 1. Channel length modulation 2. Body effect.	**6**	2:1:1.6.1
	b.	What is a noise margin? Obtain the values of VIL, VOL, VIH and VOH from transfer characteristics of a typical inverter.	**6**	2:1:1.6.1
	c.	Explain the ideal IV characteristics of nMOS transistor. Derive the equation for I_{DS} Cut off, Linear and Saturation region	**8**	2:1:1.6.1
		OR		
2.	**a.**	With neat diagram, explain the nMOS fabrication steps.	**6**	2:1:1.6.1
	b.	Compare Bipolar and CMOS technology.	**6**	2:1:1.6.1
	c.	Explain the CMOS inverter transfer characteristics by highlighting the regions of the MOS transistor.	**8**	2:1:1.6.1
		Module-2		
3.	**a.**	Explain with circuit diagram the super buffers with inverting type and non-inverting type of nMOS.	**6**	2:1:1.6.1
	b.	Draw the schematic, stick diagram and Layout for 2 input CMOS NOR gate.	**6**	2:2:1.6.1
	c.	Derive expressions for rise time and fall time for 1:1 CMOS inverter.	**8**	3:1:1.7.1
		OR		
4.	**a.**	What are the different MOS Layers? Discuss the λ based design rules for layers and transistors.	**6**	2:2:1.6.1
	b.	Calculate the area capacitance values associated with the following structure, having different layers as shown in figure 4.1.	**6**	3:2:1.7.1

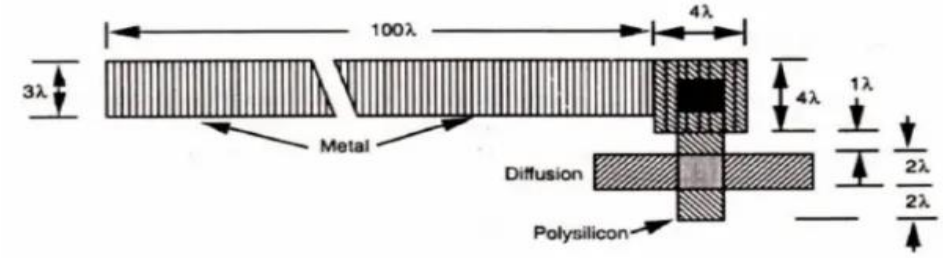

Fig 4.1

Note: relative "C' value for polysilicon-to-substrate=0.1 pf x $10^{-4}/\mu m^2$ and metal1-to-substrate=0.075 pf x $10^{-4}/\mu m^2$.

Note: (RBTL - Revised Bloom's Taxonomy Level: CO - Course Outcome: PI – Programme Outcome)

	c.	Derive the expression for total delay for N stage of NMOS and CMOS inverters by assuming the width factor f=e.	**8**	3:2:1.7.1

Module-3

5.	**a.**	Derive the scaling factor for the following parameter 1. Channel resistance. 2. Parasitic capacitance. 3. Gate delay.	**6**	3:1:1.7.1
	b.	Explain carry select adder with neat block diagram.	**6**	2:2:1.6.1
	c.	Explain dynamic and Domino logic families with its advantages and disadvantages.	**8**	2:2:1.6.1

OR

6.	**a.**	With truth table explain the operation of 2 input NAND using pseudo nMOS logic.	**6**	2:2:1.6.1
	b.	With relevant diagram discuss Manchester carry chain operation.	**6**	2:2:1.6.1
	c.	Explain ALU functions like EX-OR, EX-NOR, AND and OR operations with an adder. Draw the block diagram of 4-bit ALU using adder element.	**8**	2:2:1.6.1

Module-4

7.	**a.**	Explain the following logics 1. clocked CMOS logic 2.n-p CMOS logic	**6**	2:2:1.6.1
	b.	Draw the block diagram of generic structure of FPGA fabric and explain it.	**6**	2:4:1.6.1
	c.	Explain parity generator with NMOS implementation with stick diagram.	**8**	2:2:1.6.1

OR

8.	**a.**	Discuss the architectural issues related to VLSI sub system design.	**6**	2:2:1.6.1
	b.	Explain the goals and techniques of FPGA based system design.	**6**	2:4:1.6.1
	c.	Explain 4-way data selector (multiplexer) with Boolean expression and nMOS stick diagram.	**8**	2:2:1.6.1

Module-5

9.	**a.**	Explain scan-based design with necessary diagrams.	**6**	2:5:1.6.1
	b.	What are the requirements for system timing considerations.	**6**	2:3:1.6.1
	c.	Explain 3 transistor dynamic RAM cell with schematic diagram.	**8**	2:3:1.6.1

OR

10	**a.**	Explain logic verification principles.	**6**	2:5:1.6.1
	b.	Explain nMOS pseudo static RAM cell with its schematic.	**6**	2:3:1.6.1
	c.	Explain the following 1. Ad hoc testing 2. BIST	**8**	2:5:1.6.1

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