Basavarajeswari Group of Institutions

BALLARI INSTITUTE OF TECHNOLOGY & MANAGEMENT

(Autonomous Institute under Visvesvaraya Technological University, Belagavi)

USN										

Course Code **22CS/AI/CA/CD/32**

Third Semester B.E. Degree Examinations, March/April 2024

DIGITAL SYSTEM DESIGN AND COMPUTER ORGANIZATION

(Common to CSE, AIML, CSE- AI, CSE- DS)

Duration: 3 hrs **Max. Marks: 100**

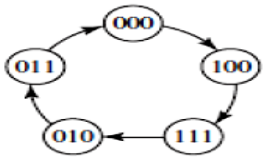
Note: 1. Answer any* FIVE *full questions choosing ONE full Question from each Module.
2. Missing data, if any, may be suitably assumed

Q. No		*Question*	*Marks*	*(RBTL:CO: PI)*
		Module-1		
1.	**a.**	Solve the following SOP(Minterms) functions using K-Map: **f(A, B,C,D)= ∑m(1,5,6,7,11,12,13,15)** **f(A, B,C,D)= ∑m(6,7,9,10,13) + d(1,4,5,11)**	**07**	(3 :1: 1.7.1)
	b.	Solve the following POS(Maxterms) functions using K-Map: **f(A, B,C,D)= πM(0,2,3,8,9,12,13,15)** **f(A, B,C,D)= πM(1,2,3,4,9,10) . d (0,15)**	**07**	(3 :1: 1.7.1)
	c.	Find all prime implicants and all minimum sum-of-products expressions using K-map: - **f (A, B, C, D) = A`B+B`C+ABCD`**	**06**	(3 :1: 1.7.1)
		(OR)		
2.	**a.**	Solve using Map entered variable use four variable Map to find minimum SOP **Z(A, B,C,D,E,F)=∑m(0,2,3,11,15)+∑d(1,10,13)+ E(m5+m7)+F(m9)**	**07**	(3 :1: 1.7.1)
	b.	Identify all essential prime implicants using **QM Method** and prime implicants chart **F (a, b, c, d) = ∑m(0,1,2,3,8,9)**	**07**	(3 :1: 1.7.1)
	c.	Solve the below function using MEV technic and draw reduced circuit using basic gates: - f **(A, B, C,D)=Σm(1, 2, 4, 5,6,8,9,11, 15)+Σd(3, 7, 13)**	**06**	(3 :1: 1.7.1)
		Module-2		
3.	**a.**	(i)What is multiplexer? Explain **4:1 MUX** along with truth table and circuit diagram. (ii) Realize f (A, B, C) = ∑m(0,1,3,5) using 4:1 Mux.	**07**	(2:2: 1.7.1)
	b.	Show how two 2-to-l multiplexers could be connected to form a 3-to-l MUX. Input selection should be as follows: If AB = 00, select I0, If AB = 01, select I1, If AB = 1 -(B is a don't-care), select I2. Show how two 4-to-l and one 2-to-1mulliplexers could be connected to form an 8-to-1 MUX with three control inputs	**07**	(2 :2: 1.7.1)
	c.	What is decoder? Explain 3:8 Decoder along with truth table and circuit diagram.	**06**	(2 :2: 1.7.1)
		(OR)		
4.	**a.**	Build a Full adder using a 3-to-8-line Decoder using: (i) Two OR gates. (ii) Two NOR gates.	**07**	(2 :2: 1.7.1)
	b.	Explain J K flip flop along with characteristics equation.	**07**	(2 :2: 1.7.1)

Note: (RBTL - Revised Bloom's Taxonomy Level: CO - Course Outcome: PI– Performance Indicator)

	c.	Implement a Full Adder and Full Subtractor using a PAL.	**06**	(3 :2: 1.7.1)

Module-3

5.	**a.**	Explain 8-bit serial-in, serial-out shift registers along with timing diagram.	**07**	(2 :3: 1.7.1)
	b.	Design MOD-8 counter J K Flip Flops.	**07**	(3 :3: 1.7.1)
	c.	Design counter for the following counting sequence: 	**06**	(3 :3: 1.7.1)

(OR)

6.	**a.**	Explain data transfer between registers with example.	**07**	(2 :3: 1.7.1)
	b.	Design MOD-5 Counter using JK flip-flop.	**07**	(3 :3: 1.7.1)
	c.	Explain sequential parity checker with state diagram and table.	**06**	(2 :3: 1.7.1)

Module-4

7.	**a.**	Explain steps of basic operational concepts of computer for ADD LOCA, R1, with neat diagram.	**07**	(2 :4: 1.7.1)
	b.	Explain single Bus structure.	**07**	(2 :4: 1.7.1)
	c.	Explain Big-Endian and Little-Endian. Show the content of the two memory words at address 1000 and 1004 after the name ***"BITM, BALLARI"*** has been entered in both methods.	**06**	(2 :4: 1.7.1)

(OR)

8.	**a.**	Explain the following addressing modes with examples. (i) Register (ii) Direct (iii) Indirect	**07**	(2 :4: 1.7.1)
	b.	Solve and explain Y= (A+B) *(C+D) using one-address, two-address, three-address instructions.	**07**	(3 :4: 1.7.1)
	c.	Explain conditional codes (Flag Register).	**06**	(2 :4: 1.7.1)

Module-5

9.	**a.**	Explain the registers used in keyboard and display	**07**	(2 :5: 1.7.1)
	b.	Explain handling multiple devices: (i) Vectored interrupt and interrupt nesting. (ii) simultaneous request (daisy chain, arrangement of priority groups)	**07**	(2 :5: 1.7.1)
	c.	What is DMA? What are it advantages? With supporting diagram, explain different registers used in DMA interface.	**06**	(2 :5: 1.7.1)

(OR)

10	**a.**	What is bus Arbitration? Explain centralized Arbitration.	**07**	(2 :5: 1.7.1)
	b.	Explain logic diagram 4-bit carry look ahead adder (Design of Fast adder)	**07**	(2 :5: 1.7.1)
	c.	Apply booth algorithm to perform the multiplication on -13 and -04.	**06**	(3 :5: 1.7.1)

** ** **

Note: (RBTL - Revised Bloom's Taxonomy Level: CO - Course Outcome: PI– Performance Indicator)