`Basavarajeswari Group of Institutions

BALLARI INSTITUTE OF TECHNOLOGY & MANAGEMENT

(Autonomous Institute under Visvesvaraya Technological University, Belagavi)

USN											Course Code	2	1	E	C	3	3

Third Semester B.E. Degree Examinations, April/May 2023

DIGITAL CIRCUIT DESIGN USING VERILOG

Duration: 3 hrs **Max. Marks: 100**

Note: ***1. Answer any* FIVE *full questions, choosing* ONE *full question from each module.***
2. Missing data, if any, may be suitably assumed

Q. No		*Question*	*Marks*	*(RBTL:CO:PI)*
		MODULE – 1		
1.	**a.**	Simplify the following using K-Map (Karnaugh Map) $f(A,B,C,D) = \sum m(0,2,3,8,10,11,12,14)$	**06**	(3 :1 : 1.7.1)
	b.	(i) Convert from SOP to canonical SOP: $f = A\overline{B} + A\overline{C} + BC$ (ii) Convert from POS to canonical POS : $f = (A+\overline{B}) \bullet (\overline{B}+C)$	**06**	(2 :1 : 1.6.1)
	c.	A four-bit binary character is presented to a circuit that must detect whether the input is a legitimate BCD code. If a non-BCD code is entered, the output is to be true. Determine the truth table and expression. Simplify and draw the circuit.	**08**	(4 :1 : 1.7.1)
		OR		
2.	**a.**	Define (i) Literals (ii) Minterm (iii) Maxterm (iv) SOP (v) Canonical SOP (vi) Canonical POS	**06**	(2 :1 : 1.6.1)
	b.	Simplify the following using 1-variable MEV map $f(A,B,C,D) = \sum m(2,3,4,5,13,15) + \sum d(8,9,10,11)$	**06**	(3 :1 : 1.7.1)
	c.	Four soldiers, A, B, C and D, volunteer to perform an important military task if any one of the following conditions are satisfied. (i) Either A or B or both must go. (ii) Either both A and C go or neither goes. (iii) If B goes then A and D must also go. Determine the expression that specifies the combinations of volunteers that can get the assignment. Simplify and draw the circuit.	**08**	(4 :1 : 1.7.1)
		MODULE – 2		
3.	**a.**	Explain typical design flow for designing VLSI IC circuit with the help of appropriate flow diagram.	**06**	(2 :4 : 1.6.1)
	b.	Write the following numbers in appropriate format for Verilog coding: (i) Decimal number 123 as a sized 8-bit number in binary. Use _ for readability. (ii) A 16-bit hexadecimal unknown number with all x's. (iii) A 4-bit negative 2 in decimal. Write the 2's complement form for this number. (iv) An unsized hex number 1234, 8FF. (v) An unsized octal number 765, 123 (vi) 3-bit binary number with MSBs 10 and least significant bit (LSB) unknown.	**06**	(2 :4 : 1.6.1)

Note: (**RBTL - Revised Bloom's Taxonomy Level: CO - Course Outcome: PI - Performance Indicator)**

c. Write Verilog code for 2-to-1 multiplexer using bufif0 and bufif1 gates as shown in Fig. Q3 (c). **08** (3 :4 : 1.7.1)

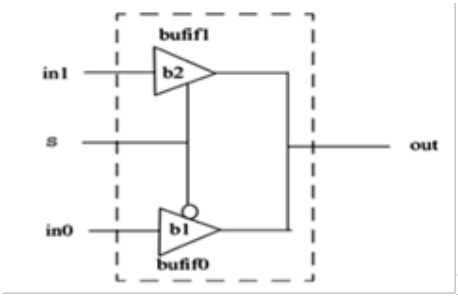

Fig. Q3 (c)

OR

4. **a.** Explain digital design methodologies with block diagram. **06** (2 :4 : 1.6.1)

b. An interconnect switch (IS) contains the following components, a shared memory (MEM), a system controller (SC) and a data crossbar (Xbar). Define the modules MEM, SC, and Xbar, using the module/end module keywords. You do not need to define the internals. Assume that the modules have no terminal lists. **06** (2 :4 : 1.6.1)

c. Write the output of following: **08** (2 :4 : 1.7.1)

a. initial
begin
$display ("Set = %b \t Reset= %b \t Q = %b \n", set, reset, q);
set = 0; reset = 0;
#5 reset = 1;
#5 reset = 0;
#5 set = 1;
end

b. Are the following statements legal strings? If not, write the correct strings.
(i) "Please ring a bell \007"
(ii) "This is a backslash \ character\n"

MODULE – 3

5. **a.** Define the following in your own words **06** (2 :2 : 1.6.1)
(i) Fan out (ii) I_{ccH} (iii) V_{oH} (iv) T_{pLH} (v). I_{os} (vi). V_{IH}

b. Draw the logic symbol for a 3-to-8 logic decoder that has active low data inputs, an active high enable, and active low data outputs. Use such a decoder to realize the Boolean equation. **06** (3 :2 : 1.7.1)
$X = f(a,b,c) = \sum m(0,3,5,6)$

c. Sketch the logic symbol for a 10-line to BCD encoder. Show how 10 events can be encoded into a four-bit data bus with the help of truth table. **08** (3 :2 : 1.7.1)

OR

6. **a.** Realize the following Boolean functions using the appropriate multiplexer when a single variable MEV is permitted. **06** (3 :2 : 1.7.1)
$y = f(a,b,c,d) = \sum m(0,3,4,5,7,9,13,15)$

b. Write a note on tristate buffer. **06** (2 :2 : 1.6.1)

c. Design a two digit BCD adder using 74LS83. Also write the logic equations for a four stage look ahead carry adder in terms of data and carry inputs. **08** (3 :2 : 1.7.1)

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MODULE – 4

7.	**a.**	Draw the logic diagram. Construct the excitation table and write the characteristic equation for (i) D Flip-flop (ii) T flip-flop	**06**	(2 :3 : 1.6.1)
	b.	Define following state machine notations: (i) Input variable (ii) State variable (iii) Excitation variable (iv) State (v) Present state (vi) Next state	**06**	(2 :3 : 1.6.1)
	c.	Design asynchronous divide by 2 and divide by 4 counter using JK flip flops.	**08**	(3 :3 : 1.7.1)
		OR		
8.	**a.**	Sketch the model diagrams for a Mealy and Moore sequential circuit. Describe the difference between Mealy and Moore circuits using model diagrams.	**06**	(2 :3 : 1.6.1)
	b.	Explain the following: (i) SISO shift register (ii) PIPO shift register.	**06**	(2 :3 : 1.6.1)
	c.	Design 3-bit asynchronous divide by 8 counter using JK flip flops.	**08**	(3 :3 : 1.7.1)

MODULE – 5

9.	**a.**	Write a Verilog dataflow description for 4:1 multiplexer using logic equation.	**06**	(3 :4 : 1.7.1)
	b.	Write a Verilog code to detect a pattern 101(MSB first) using Mealy circuit.	**08**	(3 :3 : 1.7.1)
	c.	Differentiate between the following operators used in Verilog with an example (i) Logical and reduction operators (ii) concatenation and replication operators (iii) equality and case equality operators.	**06**	(3 :4 : 1.6.1)
		OR		
10.	**a.**	Differentiate between initial and always statements with example.	**06**	(3 :4 : 1.6.1)
	b.	Explain delay based timing controls with appropriate examples.	**06**	(2 :4 : 1.6.1)
	c.	Write a Verilog code to detect a pattern 101 (MSB first) using Moore circuit.	**08**	(3 :3 : 1.6.1)

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