

BALLARI INSTITUTE OF TECHNOLOGY & MANAGEMENT

(Autonomous Institute under Visvesvaraya Technological University, Belagavi)

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Course Code

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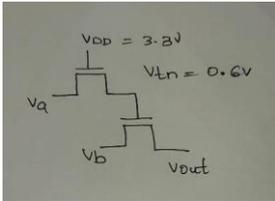
Sixth Semester B.E. Degree Examinations, September/October 2024

FUNDAMENTALS OF VLSI DESIGN

Duration: 3 hrs

Max. Marks: 100

Note: 1. Answer any FIVE full questions choosing ONE full Question from each Module.
2. Missing data, if any, may be suitably assumed

<u>Q. No</u>	<u>Question</u>	<u>Marks</u>	<u>(RBTL:CO:PI)</u>								
<u>Module-1</u>											
1.	a. Explain the steps involved in p-well fabrication process of CMOS inverter with relevant diagrams.	08	(2:1:1.6.1)								
	b. Derive the drain current equation of nMOSFET in linear region and analyze the same in saturation region	08	(3:1:1.7.1)								
	c. Explain the Channel Length Modulation	04	(2:1:1.6.1)								
(OR)											
2.	a. Explain the brief theory of MOS transistors? With the help of lattice clearly show the formation of p – mos and n – mos structures.	08	(2:1:1.6.1)								
	b. Explain the steps involved in twin – tub fabrication process of CMOS inverter with relevant diagrams	08	(2:1:1.6.1)								
	c. Explain velocity saturation and mobility degradation	04	(2:1:1.6.1)								
<u>Module-2</u>											
3.	a. Derive expressions for rise time and fall time for 1:1 CMOS inverter.	08	(3:2:1.7.1)								
	b. Draw the schematic, stick diagram and layout for 2 input CMOS NAND gate.	08	(3:2:1.7.1)								
	c. Differentiate buried and butting contact with suitable diagrams.	04	(2:2:1.6.1)								
(OR)											
4.	a. What are the different MOS layers? Draw the lambda-based design rules for layers and transistors.	08	(2:2:1.6.1)								
	b. Calculate the output of voltage V_{out} in the circuit shown in Fig. Q4(b) for different values of V_a , V_b	06	(3:2:1.7.1)								
	<table border="1" style="display: inline-table; border-collapse: collapse; margin-right: 20px;"> <tr><td style="padding: 2px;">V_a</td><td style="padding: 2px;">V_b</td></tr> <tr><td style="padding: 2px;">3.3</td><td style="padding: 2px;">3.3</td></tr> <tr><td style="padding: 2px;">3.3</td><td style="padding: 2px;">1.5</td></tr> <tr><td style="padding: 2px;">1.5</td><td style="padding: 2px;">1.5</td></tr> </table> 	V_a	V_b	3.3	3.3	3.3	1.5	1.5	1.5		
V_a	V_b										
3.3	3.3										
3.3	1.5										
1.5	1.5										
	c. Explain with circuit diagram the super buffers with inverting type and non- inverting type of nMOS.	06	(2:2:1.6.1)								

Module-3

5. a. What do you mean by scaling? Explain the 10 scaling factors for device parameters? **10** (2:3:1.6.1)
b. Explain the adder enhancement techniques. Explain Manchester carry chain adder and carry skip adder. **10** (2:3:1.6.1)

(OR)

6. a. Explain the design of an ALU Subsystem with an example of 4 – bit adder **10** (3:3:1.7.1)
b. Explain the carry select adder with the help of block diagram. **10** (3:3:1.7.1)

Module-4

7. a. Explain the switch logic with an example. **10** (2:4:1.6.1)
b. Explain the parity generator with an example. **10** (2:4:1.6.1)

(OR)

8. a. Explain Programmable Logic Array (PLA) with the help of two-phase clocking. **10** (2:4:1.6.1)
b. Briefly explain the architecture of FPGA. **10** (2:4:1.6.1)

Module-5

9. a. Explain Three – Transistor and One – Transistor dynamic RAM Cell. **10** (2:5:1.6.1)
b. Explain the manufacturing test principles. **10** (2:5:1.6.1)

(OR)

- 10 a. Explain Built-in Self-Test with the help of Pseudo random sequence generator. **10** (2:5:1.6.1)
b. With the help of block diagram explain four transistor dynamic and six transistor static CMOS memory cells. **10** (2:5:1.6.1)

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