Basavarajeswari Group of Institutions
BALLARI INSTITUTE OF TECHNOLOGY & MANAGEMENT
(Autonomous Institute under Visvesvaraya Technological University, Belagavi)

| USN | | | | | | | | | | Course Code | 2 | 1 | E | C | 6 | 5 | 2 |

Sixth Semester B.E. Degree Examinations, September/October 2024
EMBEDDED SYSTEM DESIGN

Duration: 3 hrs   **Max. Marks: 100**

*Note: 1. Answer any **FIVE** full questions choosing ONE full Question from each Module.*
          2. Missing data, if any, may be suitably assumed

Q. No		*Question*	*Marks*	*(RBTL:CO:PI)*
		MODULE – 1		
1.	a	With the neat flow chart, explain the process of embedded system design and development.	10	(2:1:1.6.1)
	b	With a block diagram, explain the digital signal processor based system.	10	(2:1:1.6.1)
		(OR)		
2.	a	Describe the major blocks of embedded hardware core and a typical bus structure comprising Address, Data and control signal.	10	(2:1:1.6.1)
	b	Explain instruction and the action included in instruction with some common instruction.	10	(2:1:1.6.1)
		MODULE – 2		
3.	a	Define memory? Explain the classification of memory.	10	(2:2:1.6.1)
	b	With the neat circuit and timing diagram, explain the ROM overview.	10	(2:2:1.6.1)
		(OR)		
4.	a	With the neat circuit and timing diagram, explain the DRAM Overview.	10	(2:2:1.6.1)
	b	Define the following: (i) The access time (ii) The cycle time (iii) Block Size (iv) Latency (v) Block Access Time	10	(2:2:1.6.1)
		MODULE – 3		
5.	a	Explain the SPI bus interfacing and sequence of operation for communicating with a SPI device.	10	(2:3:1.6.1)
	b	With the neat interface diagram, explain on board I2C communication bus.	10	(2:3:1.6.1)
		(OR)		
6.	a	Describe the elements of an embedded system with a block diagram.	10	(2:3:1.6.1)
	b	Differentiate between (i) Embedded System and general computing system (ii) RISC and CISC	10	(2:3:1.6.1)
		MODULE – 4		
7.	a	Explain the steps in detail that comprise the V-life cycle model.	10	(2:4:1.6.1)
	b	In detail, explain the five steps to a successful design for problem solving.	10	(2:4:1.6.1)

Note: (RBTL - Revised Bloom's Taxonomy Level: CO - Course Outcome: PI– Performance Indicator)

8.	a	Explain the process of identifying the requirements that interface between the customer and design process.	**10**	**(2:4:1.6.1)**
	b	Define life cycle model and its objectives. With the neat diagram, explain waterfall life- cycle model.	**10**	**(2:4:1.6.1)**

<u>MODULE – 5</u>

9.	a	With a neat block diagram, explain the major components of operating system.	**10**	**(2:5:1.6.1)**
	b	Define threads. With a neat block diagram, explain a single thread and multiple threads.	**10**	**(2:5:1.6.1)**

(OR)

10.	a	Differentiate between (i) Process and Threads (ii) Program and process	**10**	**(2:5:1.6.1)**
	b	With a neat block diagram and C code fragment, explain the task control block.	**10**	**(2:5:1.6.1)**

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