USN											Course Code	2	2	E	E	3	2

Third Semester B.E. Degree Examinations, September 2024
DIGITAL ELECTRONICS

Duration: 3 hrs   **Max. Marks: 100**

Note: *1. Answer any* **FIVE** *full questions choosing ONE full Question from each Module.*
        2. Missing data, if any, may be suitably assumed

Q. No		*Question*	*Marks*	*(RBTL:CO:PI)*
		Module-1		
1.	a.	Explain following terms with examples: (i) Literal (ii) SOP term and POS term (iii) Minterm and Maxterm (iv) Canonical SOP (v) Canonical POS	**10**	(2 :1 : 1.3.1)
	b.	Determine all the minimal expression for the following function using Karnaugh maps and mark prime implicants and essential prime implicants. R= $f(v, w, x, y, z)$=∑m(5,7,9,12,13,14,15,20,21,22,23,25,29,31)	**10**	(3 :1 : 2.1.2)
		(OR)		
2.	a.	Explain the design steps in combinational logic with neat diagram.	**10**	(2 :1 : 1.3.1)
	b.	Determine minimal SOP expression using Quine-McCluskey method. M=$f(a, b, c, d)$= ∑m(0,5,6,7,9,10,12,15)	**10**	(3 :1 : 2.1.2)
		Module-2		
3.	a.	Explain the followings: (i) Decoders (ii) Encoders.	**10**	(2 :2 : 1.3.1)
	b.	Implement the following Boolean functions using 3-8 line decoder IC74138 with active low outputs and logic gates. (i) F1=$f(x, y, z)$= x'y'z'+ x'yz'+ xy'z'+xyz' F2=$f(x, y, z)$=ΠM(0,1,3,5,7). (ii) F1=$f(a ,b, c, d)$=∑(1,4,6,10) F2=$f(a, b ,c, d)$=ΠM(3,5,13,15).	**10**	(3 :2 : 2.1.2)
		(OR)		
4.	a.	Explain look ahead carry generation using full adder and construct 4-bit adder with look ahead carry scheme.	**10**	(2 :2 : 1.3.1)
	b.	Implement the $Z = f(w, x, y, z)$= ∑(0,1,2,4,7,9,12,14) function using: (i) 8:1 MUX (ii) 4:1 MUX	**10**	(3 :2 : 2.1.2)
		Module-3		
5.	a.	Explain the Sequential circuits with neat block diagram.	**06**	(2 :3 : 1.3.1)
	b.	Explain the SR latch with logic diagram, symbol and truth table.	**06**	(2 :3 : 1.3.1)
	c.	Explain the working of JK Flip-Flop with neat diagram, truth table and waveforms.	**08**	(2 :3 : 1.3.1)
		(OR)		
6.	a.	Obtain the characteristics equations for SR flip flop, JK flip flop.	**06**	(2 :3 : 1.3.1)
	b.	Explain the race around condition with the help of waveforms.	**06**	(2 :3 : 1.3.1)
	c.	Explain the Master-Slave SR flip flop with logic diagram, symbol, truth table and timing diagram.	**08**	(2 :3 : 1.3.1)

Note: (RBTL - Revised Bloom's Taxonomy Level: CO - Course Outcome: PI– Performance Indicator)

Module-4

7. **a.** Explain SISO, SIOP, PISO, and PIPO shift operations with relevant diagrams. **10** (2 :4 : 1.3.1)

    b. Design synchronous MOD-5 counter using clocked JK flip flop for the sequence 1→2→6→0→5→ again 1→2→….. **10** (3 :4 : 2.1.2)

(OR)

8. **a.** Explain working of 4-bit asynchronous UP/DOWN counter. **10** (2 :4 : 1.3.1)

    b. Design synchronous MOD-6 counter using clocked T flip flop for the sequence 5→4→3→0→7→2→ again 5→4→….. **10** (3 :4 : 2.1.2)

Module-5

9. **a.** Explain the state machine notations. **08** (2 :5 : 1.3.1)

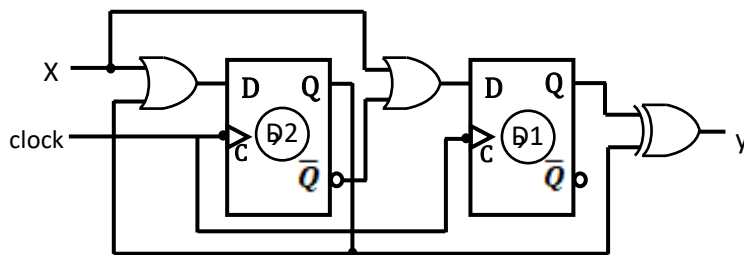   **b.** Construct state table and state diagram for the circuit shown in Fig.9.b. **12** (3 :5 : 2.1.2)

Fig.9.b

(OR)

10 **a.** Distinguish between Moore and Mealy models. **08** (2 :5 : 1.3.1)

    b. A sequential circuit has one input and one output, the state diagram shown in Fig.10.b, design sequential circuit using JK Flip Flops. **12** (3 :5 : 2.1.2)
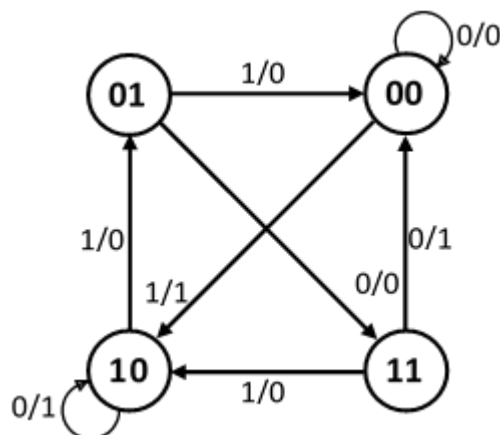

Fig.10.b

** ** **

Note: (RBTL - Revised Bloom's Taxonomy Level: CO - Course Outcome: PI– Performance Indicator)