

USN Course Code

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Third Semester B.E. Degree Examinations, September 2024

ANALOG ELECTRONIC CIRCUITS

Duration: 3 hrs

Max. Marks: 100

*Note: 1. Answer any FIVE full questions choosing ONE full Question from each Module.**2. Missing data, if any, may be suitably assumed*

| <u>Q. No</u> | <u>Question</u> | <u>Marks</u> | <u>(RBTL:CO:PI)</u> |
|------------------------|---|--------------|---------------------|
| <u>Module-1</u> | | | |
| 1. | a. Sketch and explain double ended clipper circuit | 06 | (2 : 1 : 1.4.1) |
| | b. Derive an expression for E_{th} , I_B and V_{CE} for voltage divider bias circuit using exact analysis. | 07 | (3 : 1 : 1.4.1) |
| | c. The emitter bias configuration has the following specifications $I_{CQ} = 1/2(I_{csat})$, where $I_{csat}=8mA$, $V_{CC}=28V$ and $V_c=18v$, $\beta=110$. Determine R_B , R_C and R_E | 07 | (3 : 1 : 2.4.1) |
| (OR) | | | |
| 2. | a. Draw a positive clamper circuit and explain its operation. Also draw the input and output waveforms. | 06 | (2 : 1 : 1.4.1) |
| | b. Derive an expression for the stability factor $S_{(ICQ)}$ for a collector feedback bias configuration | 07 | (3 : 1 : 1.4.1) |
| | c. Design a voltage divider bias circuit for the specified condition $V_{CC} = 12V$, $V_{CE} = 6V$, $I_C = 1mA$, $S_{(ICQ)} = 20$, $\beta = 100$, $V_E = 1V$. | 07 | (3 : 1 : 2.4.1) |
| <u>Module-2</u> | | | |
| 3. | a. Obtain the expressions for Z_i , Z_o , A_v , A_{vs} , A_i and A_{is} of CE configuration using h parameter | 10 | (3 : 2 : 1.4.1) |
| | b. State and prove Miller's theorem | 10 | (3 : 2 : 1.4.) |
| (OR) | | | |
| 4. | a. Derive an expression for lower cut off frequencies due to various RC networks in CE amplifiers | 10 | (3 : 2 : 1.4.1) |
| | b. Prove that Miller's effect of input capacitance $C_{Mi}=(1-A_v) C_f$ and output capacitance $C_{Mo}=(1-1/A_v) C_f$ | 10 | (3 : 2 : 1.4.1) |
| <u>Module-3</u> | | | |
| 5. | a. State the need of cascading in amplifiers and explain with neat sketch the n-stage cascade amplifier | 10 | (2 : 3 : 1.4.1) |
| | b. Derive an expression for Z_i , A_I and A_V for a Darlington emitter follower circuit. | 10 | (3 : 3 : 1.4.1) |

(OR)

6. a. Prove that how band width of an amplifier increases with negative feedback? **10 (3 : 3 : 1.4.1)**
 b. Derive an expression for Z_{if} and Z_{of} for a current series feedback amplifier **10 (3 : 3 : 1.4.1)**

Module-4

7. a. Explain the operation of class B push-pull amplifier. Prove that the maximum efficiency of class B configuration is 78.5 %? **10 (2 : 4 : 1.4.1)**
 b. A series fed class-A amplifier shown in Fig. Q.7(b) operates from DC source and applied sinusoidal input signal generates peak base current 9mA with $R_B=1.5k\Omega$, $R_L=16\Omega$, $V_{cc}=20V$ Calculate: (i) Quiescent current I_{CQ} , (ii) Quiescent voltage V_{CEQ} , (iii) DC input power P_{DC} , (iv) AC output power P_{ac} , (v)Efficiency. Assume $\beta=50$ and $V_{BE}=0.7 V$ **10 (3:4 : 2.1.2)**

(OR)

8. a. Explain the working and operation of Wein bridge oscillator with a neat circuit diagram **10 (2 : 4 : 1.4.1)**
 b. Explain how Barkhausen criteria is satisfied in RC phase shift oscillator and, also design RC phase shift oscillator to generate 5KHz sine wave with 20V peak to peak amplitude. Draw the designed network. Assume $h_{fe}=150$. **10 (3 : 4: 2.1.2)**

Module-5

9. a. Calculate the trans-conductance g_m of a JFET having values of $I_{DSS}=12mA$ and $V_p= - 4v$ at bias points (i) $V_{GS}=0v$ (ii) $V_{GS}= -1.5v$ **06 (3 : 5 : 2.1.2)**
 b. Derive the expressions for A_v , R_i and R_o for fixed bias circuit with common source configuration using small signal model. **07 (2 : 5 : 1.4.1)**
 c. Explain the construction, working and characteristics of an n-channel JFET. **07 (2 : 5 : 1.4.1)**

(OR)

- 10 a. A JFET has $g_m= 6m\Omega$ at $V_{GS}= -1V$. Find I_{DSS} if pinch off voltage $V_p = - 2.5V$. **06 (3 : 5 : 2.1.2)**
 b. Compare BJT and FET. **07 (2 : 5 : 1.4.1)**
 c. Draw and explain the construction of n-channel E-MOSFET **07 (2 : 5 : 1.4.1)**

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