Basavarajeswari Group of Institutions

BALLARI INSTITUTE OF TECHNOLOGY & MANAGEMENT

(Autonomous Institute under Visvesvaraya Technological University, Belagavi)

USN											Course Code	2	1	E	E	4	2

Fourth Semester B.E. Degree Examinations, September 2024

DIGITAL CIRCUITS DESIGN

Duration: 3 hrs **Max. Marks: 100**

Note: ***1. Answer any* FIVE *full questions, choosing* ONE *full question from each module.***
2. Missing data, if any, may be suitably assumed.

Q. No		*Question*	*Marks*	*(RBTL:CO:PI)*
		MODULE – 1		
1.	**a.**	Derive the following expressions in the canonical form: $f(w,x,y,z) = wxy + wxz + wyz + wx + \bar{y}\bar{z}$	**10**	(3 :1 : 2.1.2)
	b.	Determine the SOP expression for the following Boolean function using K-map and draw the logic diagram f(a, b, c, d) = Σm (0,1,2,3,4,5,8,9,10,11,12,14) + Σd (6,15)	**10**	(3 :1 : 2.1.2)
		OR		
2.	**a.**	Determine essential prime implicates for the following Boolean functions using K-map f(a, b, c, d, e) = πM (0,1,2,3,8,9,10,11,16,18,20,21,22,23,24,26,28,30)	**10**	(3 :1 : 2.1.2)
	b.	Determine all PI and EPI for the following functions using Quine-McCluskey method f(w, x, y, z) = ∑m (1,3,13,15) + dc (8,9,10,11)	**10**	(3 :1 : 2.1.2)
		MODULE – 2		
3.	**a.**	Explain the general structure of decoder with block diagram.	**04**	(2 :2 : 1.3.1)
	b.	Design 4-bit binary to gray code converter combinational logic circuit using Ex- OR Gate 7486 IC.	**10**	(3 :2 : 2.1.2)
	c.	Design 4:2 priority encoder, represent truth table, switching equations, k-maps and logic diagram.	**06**	(3 :2 : 2.1.2)
		OR		
4.	**a.**	Implement following multiple output function using 74138IC and external gates F1=f(a, b, c, d) = ΠM (3,5,6,7,11,13,14,15) F2=f(a, b, c, d) = Σm (1,2,4,7,9,10,12,15)	**10**	(3 :2 : 2.1.2)
	b.	Implement the Z = f(w, x, y, z) = ∑m(0,3,5,7,9,10,11,12,14,15) function using 4:1 MUX, consider y, z as select inputs.	**06**	(3 :2 : 2.1.2)
	c.	Explain problem in a parallel adder.	**04**	(2 :2 : 1.3.1)
		MODULE – 3		
5.	**a.**	Distinguish between sequential circuits and combinational circuits.	**04**	(2 :3 : 1.3.1)
	b.	Explain the followings with logic diagram, symbol and truth table: (i) SR latch (ii) Gated D latch	**08**	(2 :3 : 1.3.1)
	c.	Explain the working of JK Flip-Flop, represent symbol, truth table and waveforms.	**08**	(2 :3 : 1.3.1)
		OR		
6.	**a.**	Explain is '0' and '1'catching problem and how to avoid it.	**04**	(2 :3 : 1.3.1)

Note: (**RBTL - Revised Bloom's Taxonomy Level: CO - Course Outcome: PI - Performance Indicator)**

	b.	Explain master-slave SR flip flop with logic diagram, symbol, truth table and timing diagram.	**08**	(2 :3 : 1.3.1)
	c.	Derive characteristics equations for SR flip flop and JK flip flop.	**08**	(2 :3 : 1.3.1)

MODULE – 4

7.	**a.**	Explain parallel-in-serial out and parallel-in-parallel out operations.	**04**	(2 :4 : 1.3.1)
	b.	Design universal shift register to perform following functions and explain each operation.	**08**	(3 :4 : 1.3.1)

Select Lines		Register operation
S_1	S_0	
0	**0**	**Hold**
0	**1**	**Shift Right**
1	**0**	**Shift Left**
1	**1**	**Parallel Load**

	c.	Explain the 4-bit synchronous binary UP counter using positive edge triggered T flip flop.	**08**	(2 :4 : 1.3.1)

OR

8.	**a.**	Explain 2-bit binary ripple UP counter using negative edge triggered JK flip flop.	**04**	(2 :4 : 1.3.1)
	b.	Explain the Ring counter and Johnson counter and implement using 7495IC.	**08**	(2 :4 : 1.3.1)
	c.	Design synchronous MOD-8 counter using clocked D flip flop for the sequence 0→2→4→6→1→3→5→7→ again 0→2→ …….	**08**	(3 :4 : 2.1.2)

MODULE – 5

9.	**a.**	Explain Moore and Mealy models with relevant block diagrams.	**08**	(2 :5 : 1.3.1)
	b.	Construct state table and state diagram for the following sequential circuit shown in fig.9.b.	**12**	(3 :5 : 2.1.2)

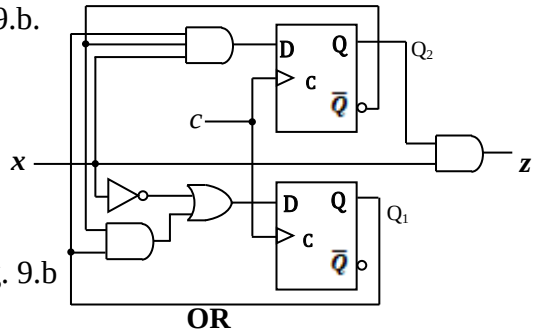

Fig. 9.b

OR

10.	**a.**	Explain state machine notations with relevant diagrams.	**08**	(2 :5 : 1.3.1)
	b.	A sequential circuit has one input and one output, the state diagram shown in fig.10.b, design sequential circuit using positive edge JK Flip Flops.	**12**	(3 :5 : 2.1.2)

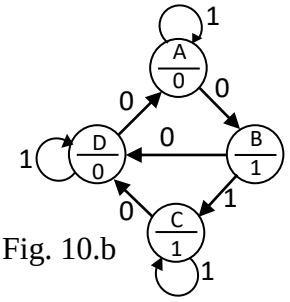

Fig. 10.b

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