Basavarajeswari Group of Institutions

BALLARI INSTITUTE OF TECHNOLOGY & MANAGEMENT

(Autonomous Institute under Visvesvaraya Technological University, Belagavi)

USN										Course Code	2	1	E	C	5	3

Fifth Semester B.E. Degree Examinations, September / October 2024

MICROCONTROLLER AND EMBEDDED SYSTEMS

Duration: 3 hrs **Max. Marks: 100**

Note: 1. Answer any* FIVE *full questions choosing ONE full Question from each Module.
2. Missing data, if any, may be suitably assumed

Q. No		Question	Marks	(RBTL:CO:PO)
		Module-1		
1.	**a.**	Give the comparisons between the following: (i) Von Neumann architecture v/s Harvard Architecture (ii) RISC v/s CISC	**06**	(2:1:1.3.1)
	b.	Explain the register organization of 8051 Microcontroller.	**07**	(2:1:1.3.1)
	c.	Give a detailed explanation on pin diagram of 8051 Microcontroller.	**07**	(2:1:1.3.1)
		(OR)		
2.	**a.**	Write a short note on following with neat diagram (i) Embedded microcontroller (ii) External memory Microcontroller	**07**	(2:1:1.3.1)
	b.	How stack operates in 8051 CPU? Discuss the need for stack memory in microcontroller?	**06**	(2:1:1.3.1)
	c.	Give the detailed memory organization of 8051 microcontroller.	**07**	(2:1:1.3.1)
		Module-2		
3.	**a.**	Illustrate with examples the different addressing modes used in 8051.	**08**	(2:2:1.3.1)
	b.	Write an ALP to exchange the source block starting with address 20H (internal RAM) containing (10) bytes of data with destination block starting with address 40H (internal RAM).	**06**	(2:2:2.1.2)
	c.	Explain the logical and bit manipulation instruction of 8051 microcontroller.	**06**	(2:2:2.1.2)
		(OR)		
4.	**a.**	Explain all the arithmetic instruction of 8051 microcontroller.	**06**	(2:2:2.1.2)
	b.	Write an ALP to perform subtraction of two 8bit numbers.	**06**	(2:2:2.1.2)
	c.	Explain the operation carried out when the following instructions are executed (i) MOVX @RO, A (ii) MOVC A, @R1+PC (iii) RLC A (iv) CJNE A,50H	**08**	(2:2:2.1.2)
		Module-3		
5.	**a.**	Explain in detail embedded software system with neat diagram of software abstraction layer executing on hardware.	**07**	(2:3:1.3.1)
	b.	Explain AMBA Bus protocol and ARM Bus technology.	**06**	(2:3:1.3.1)
	c.	Explain the register set of ARM Cortex-M3.	**07**	(2:3:1.3.1)
		(OR)		

6.	**a.**	Explain the architecture of ARM Cortex M3 in detail.	**06**	(2:3:1.3.1)
	b.	With a neat diagram explain the CPSR in detail.	**07**	(2:3:1.3.1)
	c.	Give a detailed account of different types of memories that can be used in embedded system based on hierarchy, width and type.	**07**	(2:3:1.3.1)

Module-4

7.	**a.**	Explain the working of barrel shifter with examples.	**06**	(2:4:1.3.1)
	b.	Explain MOV and MVN instructions and show the changes in the destination register after the execution of the instructions.	**06**	(2:4:2.1.2)
	c.	Explain the following logical instructions with examples: (i) AND (ii) OR (iii) EOR (iv) BIC	**08**	(2:4:2.1.2)

(OR)

8.	**a.**	Explain the following instructions with examples (i)ADD (ii) SUB (iii) RSB	**06**	(2:4:2.1.2)
	b.	Update the fields in PSW after the execution of the following instructions with examples (i) CMP (ii) CMN (iii) TST (iv) TEQ	**08**	(2:4:2.1.2)
	c.	Explain with examples (i) LSR (ii) ASR (iii) ROR	**06**	(2:4:2.1.2)

Module-5

9.	**a.**	Define embedded system. Explain the purpose of embedded system with an example for each.	**07**	(2:5:1.3.1)
	b.	Summarize the concept of (i) Bluetooth (ii) Wi-Fi	**06**	(2:5:1.3.1)
	c.	Give the difference between (i) RAM v/s ROM (ii) SRAM v/s DRAM	**07**	(2:5:1.3.1)

(OR)

10	**a.**	With a neat diagram explain the elements of embedded System	**08**	(2:5:1.3.1)
	b.	Explain how the brown –out protection circuit works.	**06**	(2:5:1.3.1)
	c.	What is the major application area of embedded system, explain with examples.	**06**	(2:5:1.3.1)

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Note: (RBTL - Revised Bloom's Taxonomy Level: CO - Course Outcome: PI– Performance Indicator)