Basavarajeswari Group of Institutions

BALLARI INSTITUTE OF TECHNOLOGY & MANAGEMENT

(Autonomous Institute under Visvesvaraya Technological University, Belagavi)

USN											Course Code	2	1	C	S	3	4

Third Semester B.E. Degree Examinations, April/May 2023

DIGITAL SYSTEM DESIGN AND COMPUTER ORGANIZATION

(Common to CSE & AIML)

Duration: 3 hrs **Max. Marks: 100**

Note: ***1. Answer any* FIVE *full questions, choosing* ONE *full question from each module.***
2. Missing data, if any, may be suitably assumed

Q. No		*Question*	*Marks*	*(RBTL:CO:PI)*
		MODULE – 1		
1.	**a.**	Solve the following functions using K-Map to find minimum SOP. Also list all essential prime implicants. f(A, B,C,D) = ∑m (1,3, 4, 11) + d (2, 7, 8, 12,14,15)	**10**	(3 :1 : 1.7.1)
	b.	Solve the following functions using K-Map to find minimum POS. Also list all essential prime implicants. f(A, B,C,D)= ∏ M(0,1,6,8,11,12). ∏ D(3,7,14,15)	**10**	(3 :1 : 1.7.1)
		OR		
2.	**a.**	Find all prime implicants using Quine McCluskey method and list all essential prime implicants using implicant chart. F (a,b,c,d) = ∑m (0,1,3,5,6,7,8,10,14,15)	**10**	(3 :1 : 1.7.1)
	b.	Using Map entered variable use four variable map to find minimum SOP Z(a,b,c,d,e,f,g) = ∑m(0,3,13,15) + ∑d(1,2,7,9,14)	**10**	(3 :1 : 1.7.1)
		MODULE – 2		
3.	**a.**	What is multiplexer? Design 8:1 MUX using two 4:1 mux and one 2:1 Mux.	**06**	(3 :2 : 1.7.1)
	b.	What is Decoder? Realize full adder using 3:8 line decoders using: (i) Two OR gates (ii) Two NOR gates	**07**	(3 :2 : 1.7.1)
	c.	Design PLA circuit for the following function: F0=∑m (0,1, 4, 6) F1=∑m (2, 3, 4, 6, 7) F2=∑m (0, 1, 2, 6) F3=∑m (2, 3, 5, 6, 7).	**07**	(3 :2 : 1.7.1)
		OR		
4.	**a.**	Implement full adder and full subtractor using a PAL.	**10**	(3 :2 : 1.7.1)
	b.	Derive characteristics equation for J K Flip-Flop, S R Flip-Flop, D Flip-Flop, and T Flip-Flop.	**10**	(3 :2 : 1.7.1)
		MODULE – 3		
5.	**a.**	Explain 8-bit serial-in, serial-out shift register using S R Flip-Flop.	**10**	(2 :3 : 1.7.1)
	b.	Construct MOD-5 counter using J K Flip-Flop.	**10**	(3 :3 : 1.1.1)
		OR		
6.	**a.**	Construct counter using JK Flip-Flop for the following counting sequence 000→100→111→010→011→000	**10**	(3 :3 : 1.7.1)
	b.	Explain a short note on : (i) Sequential parity checker (ii) Register transfers	**10**	(2 :3 : 1.7.1)

Note: (**RBTL - Revised Bloom's Taxonomy Level: CO - Course Outcome: PI - Performance Indicator)**

MODULE – 4

7.	**a.**	Explain basic operational concepts with neat diagram and example.	**08**	(2 :4 : 1.7.1)
	b.	What is performance? Give basic performance equation and overall SPEC rating of computer.	**08**	(2 :4 : 1.7.1)
	c.	Explain Big-Endian and Little-Endian. Show the content of the two memory words at address 1000 and 1004 for the name "johnson" has been entered in both methods.	**04**	(2 :4 : 1.7.1)

OR

8.	**a.**	Explain any 4 addressing modes with an example.	**08**	(2 :4 : 1.7.1)
	b.	Explain basic instruction types with an example.	**07**	(2 :4 : 1.7.1)
	c.	What is Branching? Explain with an example.	**05**	(2 :4 : 1.7.1)

MODULE – 5

9.	**a.**	Explain handling multiple devices simultaneous request(daisy chain, arrangement of priority groups)	**08**	(2 :5 : 1.7.1)
	b.	Construct a program that reads a line of characters and display it.	**05**	(3 :5 : 1.7.1)
	c.	What is DMA? What are it advantages? With supporting diagram, explain different registers used in DMA interface.	**07**	(2 :5 : 1.7.1)

OR

10.	**a.**	Explain addition and subtraction of signed numbers using 2s compliment method with an example. (i) -5 and 7 (ii) -3 and -8	**06**	(2 :5 : 1.7.1)
	b.	Construct 4 bit Carry Look Ahead adder, and unit the expression for Ci+1. And compare its performance with Ripple Bit Carry adder.	**07**	(3 :5 : 1.7.1)
	c.	Explain booth algorithm to perform the multiplication on +13 and -06.	**07**	(2 :5 : 1.7.1)

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