Basavarajeswari Group of Institutions

BALLARI INSTITUTE OF TECHNOLOGY & MANAGEMENT

(Autonomous Institute under Visvesvaraya Technological University, Belagavi)

USN											Course Code	2	2	B	E	E	2	3

Second Semester B.E. Degree Examinations, Sept/Oct-2023

BASIC ELECTRONICS

Duration: 3 hrs **Max. Marks: 100**

Note: ***1. Answer any* FIVE *full questions, choosing* ONE *full question from each module.***
2. Missing data, if any, may be suitably assumed

Q. No		*Question*	*Marks*	*(RBTL:CO: PI)*
		MODULE – 1		
1.	a.	Explain the operation of a **P-N junction** diode under forward and reverse bias condition with **V-I characteristics**.	**8**	(2:1:1.3.1)
	b.	With relevant equations explain **DC-Load Line** Analysis of a diode.	**6**	(2:1:1.3.1)
	c.	With a neat circuit diagram and waveform, explain the operation of center tapped **Full wave** rectifier.	**6**	(2:1:1.3.1)
		OR		
2.	a.	Describe the working of a **RC-π filter** for a Full Wave rectifier with neat diagram and necessary waveforms.	**8**	(2:1:1.3.1)
	b.	Explain how **Zener diode** can be used as a **voltage regulator** with load and no load.	**6**	(2:1:1.3.1)
	c.	A diode with **Vf =0.7V** is connected as a half-wave rectifier. The load resistance is **500Ω**, and the rms AC input is **22V**.Determine the following i) Peak output voltage (**Vpo**). ii) Peak Load Current **(Ip)**. iii) Diode peak reverse Voltage (**PIV**).	**6**	(2:1:1.3.1)
		MODULE – 2		
3.	a.	Draw the symbols for **npn** and **pnp** transistors and explain theterminal voltages and currents of a transistor.	**6**	(2:2:1.3.1)
	b.	Explain the **Common Emitter** configuration of a **BJT** with an **input and output VI**-characteristics	**8**	(2:2:1.3.1)
	c.	Explain concept of DC Biasing of Transistor.	**6**	(2:2:1.3.1)
		OR		
4.	a.	Draw the symbols and Structure of the following: i) N-Channel JFET ii) N-Channel **Enhancement-MOSFET** iii) N-Channel **Depletion –MOSFET**	**6**	(2:2:1.3.1)
	b.	Explain the operation of **JFET** with a neat diagram.	**6**	(2:2:1.3.1)
	c.	Explain the operation of **Enhancement-MOSFET** and Draw its Drain & Transfer characteristics.	**8**	(2:2:1.3.1)

Note: (**RBTL - Revised Bloom's Taxonomy Level: CO - Course Outcome: PI - Performance Indicator)**

MODULE – 3

5.	a.	Explain the block diagram of a Typical Op-Amp.	6	(2:3:1.3.1)
	b.	Define the following parameters. a)CMRR b)Slew Rate c)Input Offset Voltage d) Input Bias current	8	(2:3:1.3.1)
	c.	List the Characteristics of Ideal Op-Amp.	6	(2:3:1.3.1)

OR

6.	a.	Explain Op-Amp as a Voltage-Follower.	6	(2:3:1.3.1)
	b.	Explain Op-Amp as an Integrator and Differentiator.	8	(2:3:1.3.1)
	c.	Explain different Op-Amp Configurations with a neat circuit diagram.	6	(2:3:1.3.1)

MODULE – 4

7.	a.	Convert following into other number system **$010010.101100_{(2)}$**	6	(3:4:1.3.1)
	b.	Write the procedure steps of Subtraction with 2's Complement, and Using 2's Compliment subtract **$1010100_{(2)}$-$1000100_{(2)}$**	6	(3:4:1.3.1)
	c.	Convert the following expressions into **Canonical** forms: **i) f(A,B,C)=AC+AB+BC** **ii) F(A,B,C)=(A+B).(B+C).(A+C)**	8	(3:4:1.3.1)

OR

8.	a.	Define **SOP** and **POS**, and write the **expression** along with **minterm** and **Maxterm** for the given Truth Table.	6	(3:4:1.3.1)

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

	b.	Draw the **Symbols** and **Truth Table** for all **Logic Gates**	8	(2:4: 1.3.1)
	c.	Design and Draw **Full-Adder** Circuit using **Logic Gates**.	6	(3:4:1.3.1)

MODULE – 5

9.	a.	Explain the **Elements** of a **Embedded System.**	8	(2:5: 1.3.1)
	b.	Explain the **Classification of Embedded System** with a neat diagram.	6	(2:5: 1.3.1)
	c	List the Difference between **Embedded systems Vs General Computing System**.	6	(2:5: 1.3.1)

OR

10.	a.	Explain the Block Diagram of **Communication System**.	8	(2:5: 1.3.1)
	b.	Explain the different types of **Modulation Techniques**.	6	(2:5: 1.3.1)
	c.	List out the Difference between **Microprocessor Vs Microcontroller**.	6	(2:5: 1.3.1)

** *All The Best* **

Note: (**RBTL - Revised Bloom's Taxonomy Level: CO - Course Outcome: PI - Performance Indicator)**