USN											Course Code	22CS/AI/CA/CD/32

Third Semester B.E. Degree Examinations, September 2024

DIGITAL SYSTEM DESIGN AND COMPUTER ORGANIZATION

(Common to CSE, AIML, CSE- AI, CSE- DS)

Duration: 3 hrs **Max. Marks: 100**

Note:* *1. Answer any* FIVE *full questions choosing ONE full Question from each Module.
2. Missing data, if any, may be suitably assumed

Q. No		Question	Marks	(RBTL:CO:PI)
		Module-1		
1.	**a.**	Find the minimum sum-of-products expression for each function using K-maps: (i) $f(a, b, c, d) = \sum m(0, 2, 3, 4, 7, 8, 14)$ (ii) $f(a, b, c, d) = \Pi M(1, 2, 3, 4, 9, 15)$	**10**	(3 :1: 1.7.1)
	b.	Find the minimum sum of products and the minimum product of sums for the function using K-maps: $f(a, b, c, d) = \sum M(0, 1, 6, 8, 11, 12) + \sum D(3, 7, 14, 15)$	**10**	(3 :1: 1.7.1)
		(OR)		
2.	**a.**	Find the minimum sum-of-products expression for each function using Quine-McCluskey method: $F(A, B, C, D) = \sum m(2, 3, 4, 7, 9, 11, 12, 13, 14) + \sum d(1, 10, 15)$	**10**	(3 :1: 1.7.1)
	b.	Using the method of map-entered variables, use four-variable maps to find a minimum sum-of-products expression for $F(A, B, C, D, E) = \sum m(0, 4, 6, 13, 14) + \sum d(2, 9) + E(m1 + m12)$	**10**	(3 :1: 1.7.1)
		Module-2		
3.	**a.**	(i) Show how two 2-to-1 multiplexers (with no added gates) could be connected to form a 3-to-1 MUX. Input selection should be as follows: If AB = 00, select I_0 If AB = 01, select I_1 If AB = 1– (B is a don't-care), select I_2 (ii) Show how two 4-to-1 and one 2-to-1 multiplexers could be connected to form an 8-to-1 MUX with three control inputs.	**10**	(3 :2: 1.7.1)
	b.	Realize a **full subtractor** using a 3-to-8-line decoder with inverting outputs: (i) Two NAND gates. (ii) Two AND gates.	**10**	(3 :2: 1.7.1)
		(OR)		
4.	**a.**	Design **PLA** circuit for the following function: $F0==\sum m(0,1,4,6)$ $F1=\sum m(2,3,4,6,7)$ $F2=\sum m(0,1,2,6)$ $F3=\sum m(2,3,5,6,7)$.	**10**	(3 :2: 1.7.1)

	b.	Design using **PAL** a Full Adder	**10**	(3 :2: 1.7.1)

Module-3

5.	**a.**	Explain the working of a n-bit parallel adder with accumulator	**10**	(2 :3: 1.7.1)
	b.	Design and construct 3bit binary synchronous counter using TFF	**10**	(3 :3: 1.7.1)

(OR)

6.	**a.**	Describe Johnson's counter and Ring counter	**10**	(2:3: 1.7.1)
	b.	Design a counter using JK-FF for the sequence 1 →3 → 2 → 6 → 7 → 5 →4→1	**10**	(3 :3: 1.7.1)

Module-4

7.	**a.**	List basic operational steps of computer for Add LOCA, R0.	**10**	(2 :4: 1.7.1)
	b.	Solve and explain Y= (A+B) *(C+D) using one-address, two-address, three-address instructions.	**10**	(3 :4 :1.7.1)

(OR)

8.	**a.**	What is the effective address of the source operand in each of the following instructions, when the Register R1, and R2 of computer contain the decimal value 2300 and 3200? (i) Load 50(R1), R5 (ii) Move #2000, R5 (iii) Store 40(R1, R2), R5 (iv) Add –(R1), R2((v) Subtract (R2) +, R5.	**10**	(3 :4: 1.7.1)
	b.	Explain factors affecting performance of the computer? Give basic performance equation and overall SPEC rating of computer.	**10**	(2 :4: 1.7.1)

Module-5

9.	**a.**	Solve following numbers representing by 5 bits: (i) (-4) + (6) (ii) (-3) - (-7) (iii) (5) – (9) (iv) (8) +(-5)	**10**	(3 :5: 1.7.1)
	b.	What is Interrupt, ISR and Vectored Interrupts? Illustrate with example.	**10**	(2 :5: 1.7.1)

(OR)

10	**a.**	Apply booth algorithm to perform the multiplication on -11 and +07.	**10**	(3 :5: 1.7.1)
	b.	Write a program to illustrate reading one line from keyboard, storing into memory and echoing back to the display.	**10**	(3 :5: 1.7.1)

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Note: (RBTL - Revised Bloom's Taxonomy Level: CO - Course Outcome: PI– Performance Indicator)