*Basavarajeswari Group of Institutions*

# BALLARI INSTITUTE OF TECHNOLOGY & MANAGEMENT

(Autonomous Institute under Visvesvaraya Technological University, Belagavi)

| USN | | | | | | | | | | | Course Code | 2 | 1 | A | E | C | 4 | 8 | 2 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

## Fourth Semester B.E. Degree Examinations, Sep/Oct 2023

## DIGITAL SYSTEM DESIGN WITH FPGA

**Duration: 2 hrs** **Max. Marks: 100**

***Instructions to the Candidates:***

- ***All questions are compulsory***
- ***Each question carries 1 mark***
- ***Use only black ball point pen***
- ***Darkening two circles for the same question makes the answer invalid***
- ***Damaging/overwriting, using whiteners on the OMR are strictly prohibited.***

| ***Q. No*** | ***Question*** | | | |
|---|---|---|---|---|
| 1 | What does the term "digital" refer to in digital electronics? | | | |
| | a. Analog signals | b. Continuous signals | c. Discrete signals | d. Variable signals |
| 2 | How many flip-flops are required to build a 4-bit binary counter? | | | |
| | a.1 | b.2 | c.3 | d.4 |
| 3 | What is the function of a multiplexer in digital electronics? | | | |
| | a. To convert analog signals to digital signals | b. To combine multiple digital signals into one | c. To perform logical operations on digital signals | d. To synchronize digital signals |
| 4 | Which logic gate is used to implement the logical AND-NOT operation? | | | |
| | a. OR gate | b. AND gate | c. XOR gate | d. NAND gate |
| 5 | What is the key characteristic of a Mealy machine? | | | |
| | a. Outputs are dependent only on the current state | b. Outputs are dependent only on the inputs | c. Outputs are dependent on both the current state and inputs | d. Outputs are independent of both the current state and inputs |
| 6 | In a Moore machine, when are the outputs associated with the current state? | | | |
| | a. Inputs only | b. Next state only | c. Both inputs and next | d. Current state only |
| 7 | In a Moore machine, when are the outputs associated with the current state? | | | |
| | a. Inputs only | b. Next state only | c. Both inputs and next | d. Current state only |
| 8 | What is setup time in sequential circuits? | | | |
| | a. The minimum time required for the input to be stable before the clock edge | b. The time required for the output to settle after the clock edge | c. The time interval between two consecutive clock edges | d. The maximum time allowed for the input to change after the clock |
| 9 | What is hold time in sequential circuits? | | | |
| | a. The minimum time required for the input to be stable after the clock edge | b. The time required for the output to settle before the clock edge | c. The time interval between two consecutive clock edges | d. The maximum time allowed for the input to change before the |
| 10 | What is clock frequency in sequential circuits? | | | |
| | a. The number of clock cycles per second | b. The time it takes for the clock signal to transition from low to high | c. The time it takes for the clock signal to transition from high to low | d. The time it takes for the output to settle after the clock edge |
| 11 | What is the binary representation of the decimal number 13? | | | |
| | a. 1101 | b. 1001 | c. 1011 | d. 1111 |
| 12 | Which logic gate is used to perform addition in a binary adder circuit? | | | |
| | a. XOR gate | b. AND gate | c. OR gate | d. NOT gate |
| 13 | What is the purpose of a decoder in digital electronics? | | | |
| | a. To convert binary data into decimal format | b. To convert binary data into hexadecimal format | c. To convert binary data into gray code format | d. To convert binary data into an encoded format |
| 14 | Which memory element is commonly used in sequential logic circuits? | | | |
| | a. Flip-flop | b. Multiplexer | c. Decoder | d. Comparator |
| 15 | What is the main difference between combinational logic and sequential logic? | | | |

Note: (**RBTL - Revised Bloom's Taxonomy Level: CO - Course Outcome: PI - Performance Indicator)**

a.combinational logic uses memory element while sequential logic does not.

b.combinational logic generates outpu based on previous inputs, while sequentia logic does not.

c.combinational logic generates outpu solely based on the current input, whil sequential logic considers both currer

d.combinational logic perform arithmetic operations, whil sequential logic does not.

**16** Which type of machine requires fewer states to implement a given functionality?

a. Mealy machine

b. Moore machine

c. Both require the same number of states

d. It depends on the specific functionality

**17** How outputs are typically associated with states in a Mealy machine?

a. Each state has separate output bits

b. Outputs are associated with transitions between states

c. Outputs are associated with the current state only

d. Outputs are associated with the next state only

**18** What is clock skew in sequential circuits?

a. The difference in propagation delay between two paths in a circuit

b. The difference in voltage levels between the clock signal and the

c. The delay caused by clock distribution networks

d. The delay between the clock signal and the data signal

**19** What is clock period in sequential circuits?

a. The time it takes for the clock signal to transition from low to high

b. The time it takes for the clock signal to transition from high to low

c. The time interval between two consecutive clock edges

d. The time it takes for the output to settle after the

**20** What is clock frequency in sequential circuits?

a. The number of clock cycles per second

b. The time it takes for the clock signal to transition from low to high

c. The time it takes for the clock signal to transition from high to

d. The time it takes for the output to settle after the

**21** What is the setup violation in sequential circuits?

a.When the input changes after the setup time has passed

b.When the input changes before the setup time has passed

c.When the output settles after the hold time has passed

d.When the output settles before the hold time has passed

**22** What is clock gating in sequential circuits?

a. The technique used to reduce clock skew

b. The technique used to reduce power consumption by gating the clock

c. The technique used to adjust the clock period

d. The technique used to adjust the clock frequency

**23** What is clock distribution in sequential circuits?

a.The process of generating the clock signal

b.The process of distributing the clock signal to various components in the circuit

c.The process of reducing clock skew

d.The process of reducing power consumption in the clock signal

**24** What is a flip-flop?

a.A clocked sequential logic circuit

b.A combinational logic circuit

c.A memory element that stores multiple bits

d.An input/output device

**25** What is the main purpose of a clock signal in a flip-flop?

a.To trigger the flip-flop to change its state

b.To control the propagation delay of the flip-flop

c.To provide power to the flip-flop

d.To synchronize the flip-flop with other components in the circuit

**26** What is the advantage of using synchronous flip-flops in sequential circuits?

a.They have lower power consumption compared to asynchronous flip-flops

b.They have higher speed performance compared to asynchronous flip-flops

c.They have fewer states compared to asynchronous flip-flops

d.They have simpler circuitry compared to asynchronous flip-

**27** What is Verilog?

a.A programming language for designing digital systems

b.A hardware description language (HDL)

c.A software development tool

d.A circuit simulation software

**28** What is the purpose of an always block in Verilog?

a.To specify the inputs and outputs of a module

b.To describe combinational logic in a module

c.To describe sequential behavior in a module

d.To instantiate sub-modules in a design

**29** What is the purpose of the initial block in Verilog?

a.To specify the inputs and outputs of a module

b.To describe combinational logic in a module

c.To describe sequential behavior in a module

d.To initialize the values of variables and registers

**30** How are multi-bit vectors declared in Verilog?

a.using the keyword vector

b.using the keyword integer

c.using the keyword wire

d.using the keyword reg

**31** What is the purpose of a testbench in Verilog?

a.To define the behavior of a module

b.To simulate and test the functionality of a module

c.To generate the final netlist of a design

d.To generate the waveform diagram of a design

**32** Which keyword is used to specify a blocking assignment in Verilog?

a. =

b. <=

c. :=

d. ->

**33** Which operator is used for bitwise AND in Verilog?

a. +

b. &

c. ^

d. |

**34** Which operator is used for logical OR in Verilog?

a. &

b. +

c. |

d. ^

**35** What happens when multiple blocking assignments are executed in the same always block in Verilog?

a. The assignments are executed sequentially, one after the other.

b. The assignments are executed in parallel, simultaneously.

c. The assignments result in race conditions and produce unpredictable

d. The assignments are ignored, and the original values of the variables are

**36** Which statement is typically used to model combinational logic in Verilog?

a. Blocking assignment

b. Non-blocking

c. Continuous

d. Procedural

**37** What is the advantage of using non-blocking assignments in sequential logic design?

a. Non-blocking assignments allow for more efficient use of hardware | b. Non-blocking assignments eliminate the possibility of race conditions | c. Non-blocking assignments enable simulation and synthesis tools to | d. Non-blocking assignments have a faster execution time compared to

**38** What does the acronym "SPLD" stand for in the context of digital electronics?

a. Super Programmable Logic Device | b. Systematic Programmable Logic Design | c. Simple Programmable Logic Device | d. Software-Programmed Logic Design

**39** Which of the following is a common example of a Simple Programmable Logic Device?

a. Microcontroller | b. FPGA (Field-Programmable Gate Array) | c. CPLD (Complex Programmable Logic Device) | d.PAL (Programmable Array Logic)

**40** What is the primary purpose of a Simple Programmable Logic Device (SPLD)?

a.To perform complex mathematical calculations | b. To implement digital circuits and logic functions | c. To interface with analog sensors | d. To provide wireless communication

**41** What is the main advantage of using SPLDs over traditional discrete logic components?

a. Lower cost | b. Higher speed | c. Greater flexibility & programmability | d. Smaller physical size

**42** How are the logic functions implemented in a Simple Programmable Logic Device?

a.Using a fixed mask during manufacturing | b. Through the use of transistors and capacitors | c. By programming the device with specific connections | d. By embedding a microcontroller within the device

**43** Which type of logic operation is commonly implemented using SPLDs?

a.Analog-to-digital conversion | b.Floating-point arithmetic | c.Basic AND, OR, and NOT operations | d.Image processing algorithms

**44** What does the acronym "CPLD" stand for in the context of digital electronics?

a.Configurable Parallel Logic Device | b.Complex Programmable Logic Device | c.Central Processing Logic Device | d.Customized Programmable Logic Device

**45** Which of the following statements is true about CPLDs?

a.CPLDs are fixed-function devices and cannot be reprogrammed. | b.CPLDs have limited gate count and simple architecture. | c.CPLDs are primarily used for analog signal processing. | d.CPLDs are reconfigurable after programming.

**46** What is the main advantage of using CPLDs over traditional discrete logic components?

a.Lower cost | b.Higher speed | c.Greater flexibility and | d.Smaller physical size

**47** Which of the following best describes the architecture of a CPLD?

a.Arrays of programmable logic blocks interconnected by a global routing | b.A single large programmable logic block with fixed interconnections | c.A combination of analog and digital processing elements | d.Sequential logic elements interconnected in a ring topology

**48** How do CPLDs differ from FPGAs (Field-Programmable Gate Arrays)?

a.CPLDs are larger in size compared to FPGAs. | b.CPLDs are simpler and have fewer logic resources than FPGAs | c.CPLDs have fixed interconnections, while FPGAs have reconfigurable | d.CPLDs can only be programmed using hardware description languages.

**50** What does the acronym "FPGA" stand for in the context of digital electronics?

a.Field-Programmable General Array | b.Flexible Programmable Gate Array | c.Field-Programmable Gate Array | d.Fixed Programming Gate Architecture

**51** Which of the following statements is true about FPGAs?

a.FPGAs are fixed-function devices and cannot be reprogrammed. | b.FPGAs have limited gate count and simple architecture. | c.FPGAs are primarily used for analog signal processing. | d.FPGAs can be reconfigured after programming.

**52** How are logic functions implemented in a Field-Programmable Gate Array?

a.Through the use of fixed mask during manufacturing | b.By programming the device with specific connections | c.Using a high-level programming language | d.By embedding a microcontroller within the device

**53** Which of the following best describes the architecture of an FPGA?

a.Arrays of programmable logic blocks interconnected by a global routing | b.A single large programmable logic block with fixed interconnections | c.A combination of analog and digital processing elements | d.Sequential logic elements interconnected in a ring topology

**54** How do FPGAs differ from CPLDs (Complex Programmable Logic Devices)?

a.FPGAs have fixed interconnections, while CPLDs have reconfigurable | b.FPGAs are smaller in size compared to CPLDs | c.FPGAs are simpler and have fewer logic resources than CPLDs. | d.FPGAs can only be programmed using hardware description languages.

**55** What is the primary application of FPGAs?

a. Real-time video processing | b. High-performance scientific computing | c. Digital signal processing | d. Implementing glue logic and small control circuits

**56** In digital logic design, what is the primary function of a Look-Up Table (LUT)?

a.To store analog values | b.To implement complex mathematical functions | c.To perform memory operations | d.To implement combinational logic functions

**57** What does a Look-Up Table (LUT) consist of?

a.A matrix of logic gates | b.An array of flip-flops | c.A memory storage unit | d.A truth table and a memory storage unit

**58** How does a Look-Up Table (LUT) work to implement logic functions?

a.By using fixed interconnections between gates | b.By storing the results of all possible input combinations | c.By utilizing programmable transistors | d.By performing analog-to-digital conversion

**59** What is the advantage of using a Look-Up Table (LUT) for logic implementation?

a.Faster speed compared to gate-level implementation | b.Lower power consumption | c.Flexibility to implement any arbitrary function | d.Smaller physical size compared to gate-level implementation

Note: (**RBTL - Revised Bloom's Taxonomy Level: CO - Course Outcome: PI - Performance Indicator)**

**60** How is the size of a Look-Up Table (LUT) determined?

a.By the number of input variables it can accommodate | b.By the number of output variables it can accommodate | c.By the frequency of clock cycles | d.By the technology used to manufacture it

**61** Which of the following devices is best suited for implementing simple, fixed logic functions with a limited

a.CPLD (Complex Programmable Logic Device) | b.FPGA (Field-Programmable Gate Array) | c.PAL (Programmable Array Logic) | d.ASIC (Application-Specific Integrated Circuit)

**62** In comparison to PALs, CPLDs offer:

a.Higher gate counts and | b.Simpler logic functions | c.Fixed interconnections | d.Only sequential logic

**63** Which of the following devices is most suitable for implementing small to medium-sized custom logic

a.FPGA | b.ASIC | c.CPLD | c.Microcontroller

**64** Which company is known for pioneering the development of Field-Programmable Gate Arrays (FPGAs)?

a. Intel | b. Xilinx | c. Texas Instruments | d. Altera

**65** Which PLD vendor was acquired by Intel in 2015, becoming a part of their Programmable Solutions Group?

a.Xilinx | b.Lattice Semiconductor | c.Altera | d.Microchip Technology

**66** What is the fundamental building block of an FPGA?

a.Look-Up Table (LUT) | b.Flip-Flop | c.Microcontroller | d.Multiplexer

**67** Which component of an FPGA is responsible for routing signals between different logic elements?

a.Configurable Logic | b.Clock Distribution | c.Input/Output Block | d.Global Routing

**68** What is the purpose of the Configurable Logic Block (CLB) in an FPGA?

a.To store configuration data | b.To provide clock signals | c.To implement logic functions and connections | d.To interface with external memory

**69** What is the initial step in the FPGA design and verification flow?

a.RTL synthesis | b.Place and route | c.Simulation | d.Behavioral modeling

**70** What is the primary purpose of RTL synthesis in FPGA design?

a.To create a bitstream for configuration | b.To optimize the design for area and timing | c.To simulate the design | d.To perform formal verification

**71** What does "Place and route" refer to in the context of FPGA design?

a.Arranging the functional blocks on the FPGA chip | b.Verifying the logical correctness of the design | c.Simulating the design at the RTL level | d.Optimizing the design for timing and area

**72** What is the main goal of simulation in the FPGA design flow?

a.To generate the configuration bitstream | b.To verify the functionality of the design | c.To place and route the design | d.To perform high-level synthesis

**73** Which of the following is NOT a typical step in FPGA design and verification?

a.High-level synthesis | b.RTL simulation | c.Place and route | d.Microcontroller programming

**74** What is the purpose of static timing analysis (STA) in FPGA design?

To check for functional correctness of the design | To optimize the design for area | To verify the timing requirements of the design are met | To generate the configuration bitstream

**75** Which phase of FPGA design involves checking whether the design adheres to the original requirements?

a.Synthesis | b.Simulation | c.Place and Route | d.Implementation

**76** What is the purpose of testbenches in FPGA verification?

a.To measure power consumption during operation | b.To program the FPGA with the configuration bitstream | c.To simulate and apply stimulus to the design for testing | d.To physically test the FPGA's solder connections

**77** In FPGA design, what is the role of a "golden reference"?

a.A design file that is passed to the FPGA manufacturer | b.A reference clock signal used for synchronization | c.A validated and verified version of the design used for comparison | d.A specific timing constraint applied during synthesis

**78** Why is formal verification important in FPGA-based design?

a.It ensures the FPGA operates at the highest clock frequency | b.It validates the physical layout of the FPGA chip | c.It guarantees the FPGA's power consumption is optimized | d.It proves the absence of certain design errors using mathematical

**79** Which phase of FPGA design includes ensuring that the design meets specific timing requirements?

a.Simulation | b.Place and Route | c.Implementation | d.Validation

**80** What is the purpose of regression testing in FPGA verification?

a.To verify the FPGA's physical connections | b.To test the FPGA's power consumption | c.To validate the synthesis process | d.To ensure new design changes don't introduce new bugs

**81** What is Shannon's Decomposition commonly used for in FPGA design?



Note: (**RBTL - Revised Bloom's Taxonomy Level: CO - Course Outcome: PI - Performance Indicator)**

| | | | | |
|---|---|---|---|---|
| | a.Routing signals between components | b.Generating clock signals | c.implementing complex logic functions | d.Storing configuration data |
| **82** | Shannon's Decomposition is a technique used to: | | | |
| | a.Express a complex logic function as a combination of simpler logic functions | b.Optimize FPGA interconnect resources | c.Program the clock distribution network in an FPGA | d.Configure Look-Up Tables (LUTs) in an FPGA |
| **83** | In Shannon's Decomposition, what are the two fundamental operations that help break down complex | | | |
| | a.Multiplication and division | b.Addition and subtraction | c.AND operation and NOT operation | d.OR operation and XOR operation |
| **84** | Which of the following represents Shannon's Expansion Theorem? | | | |
| | a.F(A, B, C) = F(0, B, C) · A' + F(1, B, C) · A | b.F(A, B, C) = F(0, B, C) + F(1, B, C) | c.F(A, B, C) = F(0, B, C) · F(1, B, C) | d.F(A, B, C) = F(0, B, C) + F(1, B, C) · A |
| **85** | Which of the following best describes the goal of Shannon's Decomposition in FPGA design? | | | |
| | a.To increase power consumption | b.To reduce the number of flip-flops used | c.To simplify the logic while maintaining functionality | d.To improve clock speed |
| **86** | What are carry chains in FPGAs primarily used for? | | | |
| | a.Data storage | b.Signal routing | c.Arithmetic operations | d.Clock distribution |
| **87** | In FPGA carry chains, what do carry inputs and carry outputs facilitate? | | | |
| | a.Data storage | b.Memory access | c.Clock synchronization | d.Propagation of carry |
| **88** | How do carry chains in FPGAs differ from regular signal routing resources? | | | |
| | a.Carry chains are slower and less efficient | b.Carry chains are used exclusively for clock signals. | c.Carry chains are optimized for carry propagation in arithmetic operations. | d.Carry chains cannot be reconfigured. |
| **89** | How do carry chains contribute to the performance of FPGA-based arithmetic operations? | | | |
| | a.They reduce the clock frequency | b.They minimize carry propagation delays, enabling faster operations. | c.They increase power consumption. | d.They have no impact on arithmetic performance. |
| **90** | What is the primary advantage of using register chains in some FPGAs like the Altera Stratix IV? | | | |
| | a.Increased utilization of FPGA blocks | b.Reduced power consumption | c.Faster clock speeds | d.Simplified logic design |
| **91** | How do register chains in some FPGAs differ from LUT-based approaches? | | | |
| | a.Register chains use LUTs for all logic functions. | b.Register chains require more power. | c.Register chains have a separate input to the flip-flop and allow LUTs for other logic functions. | d.Register chains are slower than LUT-based approaches. |
| **92** | Which types of configurations are commonly used for cascading in FPGAs? | | | |
| | a.NAND and XOR | b.XOR and NOT | c.OR and AND | d.AND and OR |
| **93** | What is the basic block in Xilinix FPGAs called? | | | |
| | Logic Block | Slice | Macroblock | Varsatile |
| **94** | Abbreviation of CLB in a FPGA | | | |
| | Central Logic Block | Configurable Logic Block | Combinatorial Logic | Circuit Layout Block |
| **95** | What is the name Altera used for its basic logic building block in their FPGAs? | | | |
| | a.Basic Logic Unit (BLU) | b.Configurable Logic Cell | c.Logic Block (LB) | d.Programmable Logic |
| **96** | What is the name of the building block in the Microsemi Fusion architecture? | | | |
| | a.MicroBlock | b.Logic Fusion Unit (LFU) | c.VersaTile | d.Logic Integration Module |
| **97** | What is dedicated memory in FPGAs primarily used for? | | | |
| | a.Clock distribution | b.Logic element configuration | c.Storing data and facilitating memory operations | d.Implementing arithmetic operations |
| **98** | What is the primary advantage of using dedicated memory blocks in FPGAs for storage operations? | | | |
| | a.Greater flexibility | b.Lower power | c.Faster access times | d.Improved clock distribution |
| **99** | What characterizes an asynchronous read operation in embedded memory? | | | |
| | a.Data is available on the output bus after the access time, regardless of the | b.Data is available only when the clock is active. | c.Data is never available on the output bus. | d.Data is accessible only during specific clock cycles. |
| **100** | What is the primary advantage of using dedicated multipliers in FPGAs? | | | |
| | a.Reduced clock speed | b.Improved area efficiency and speed | c.Greater flexibility in multiplication operations | d.Simplified interconnect resources |



** ** **

Note: (**RBTL - Revised Bloom's Taxonomy Level: CO - Course Outcome: PI - Performance Indicator)**