Basavarajeswari Group of Institutions

BALLARI INSTITUTE OF TECHNOLOGY & MANAGEMENT

(Autonomous Institute under Visvesvaraya Technological University, Belagavi)

USN											Course Code	2	1	E	C	3	3

Third Semester B.E. Degree Examinations, March/April 2023

DIGITAL CIRCUIT DESIGN USING VERILOG

Duration: 3 hrs **Max. Marks: 100**

Note: *1. Answer any* **FIVE** *full questions, choosing* **ONE** *full question from each module.*
2. Missing data, if any, may be suitably assumed

Q. No		*Question*	*Marks*	*(RBTL:CO: PI)*
		MODULE – 1		
1.	**a.**	**Define** with examples i) Sum term ii) Minterm iii) Maxterm iv) SOP v) POS	**08**	(2 :1: 1.6.1)
	b.	i)**Convert** from **SOP** to **canonical SOP**: $f = A\bar{B} + A\bar{C} + BC$ ii) **Convert** from **POS** to **canonical POS**: $f = (A + \bar{B}).(\bar{B} + C)$	**06**	(2 :1: 1.7.1)
	c.	Four soldiers, A, B, C and D, volunteer to perform an important military task if the following conditions are satisfied. 1. Either A or B or both must go. 2. Either both A and C go or neither goes. 3. If B goes then A and D must also go. **Determine the expression** that specifies the combinations of volunteers that can get the assignment. **Simplify and draw the circuit**.	**06**	(4 :1: 1.7.1)
		OR		
2.	**a.**	Define the combinational circuit using block diagram. List the steps for designing combinational logic circuit along with its flow diagram.	**06**	(2 :1: 1.6.1)
	b.	Simplify using K-Map $f(A,B,C,D) = \sum m(0,2,3,8,10,11,12,14,15)$	**06**	(3 :1: 1.7.1)
	c.	Simplify the following using 3 variable MEV map $f(A,B,C,D) = \sum m(2,9,10,11,13,14,15)$	**08**	(3 :1: 1.7.1)
		MODULE – 2		
3.	**a.**	i) Sketch **Typical design flow** for designing VLSI IC circuit. Outline the function of each design block. ii) Describe port connection rules in a module instantiation.	**10**	(2 :4:1.6.1)
	b.	Declare the following variables in Verilog: a. An 8-bit vector net called a_in. b. A 32-bit storage register called address. Bit 31 must be the most significant bit. Set the value of the register to a 32-bit decimal number equal to 3. c. An integer called count. d. An array called delays. Array contains 20 elements of the type integer.	**04**	(3 :4: 1.7.1)
	c.	Create your own 2-input Verilog gates called my_or, my_and and my_not from 2-input nand gates.	**06**	(3 :4: 1.7.1)
		OR		
4.	**a.**	What are the basic components of a module? Which components are mandatory? Explain two classes of basic gates: and, or, Ex-or & Ex-nor gates & bufif, not gates with the help of logic symbol and truth table.	**10**	(2 :4: 1.6.1)

Note: (**RBTL - Revised Bloom's Taxonomy Level: CO - Course Outcome: PI - Performance Indicator**)

	b.	Write the following numbers: a. Decimal number 123 as a sized 8-bit number in binary. Use _ for readability. b. A 16-bit hexadecimal unknown number with all x's. c. A 4-bit negative 2 in decimal. Write the 2's complement form for this number. d. An unsized hex number 1234.	**04**	(3 :4: 1.7.1)
	c.	Write a gate level implementation in Verilog for 2-to-1 multiplexer using **bufif0** and **bufif1** gates.	**06**	(3 :4: 1.7.1)

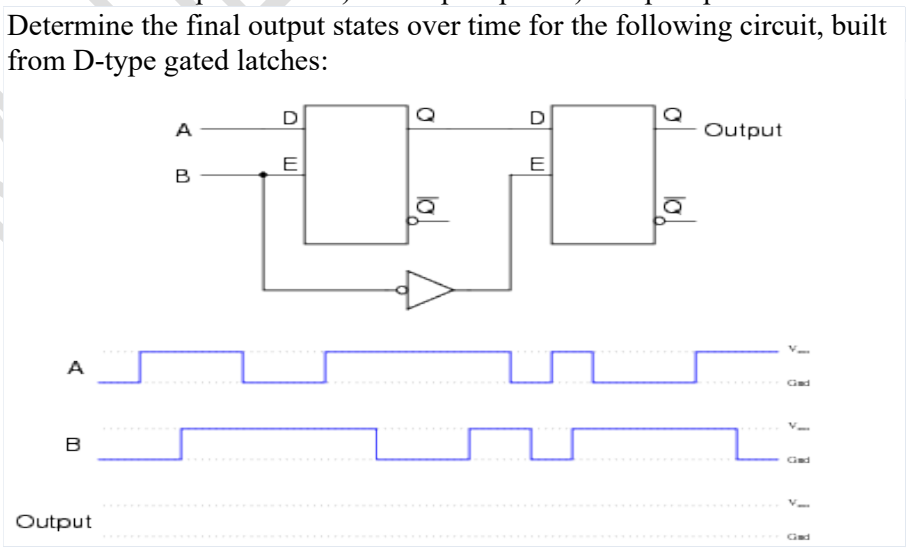
MODULE – 3

5.	**a.**	Define the following in your own words (a) Fan-out (b)Power Supply Current (c) Current Input High (d) Voltage Output High (e) Voltage Input Low (f) Propagation Delay time from output low to high	**06**	(1 :2: 1.6.1)
	b.	Sketch the logic symbol for a **10 line to BCD encoder**. Show how 10 events can be encoded into a 4-bit data bus.	**06**	(3 :2:1.7.1)
	c.	Realize the following Boolean function using appropriate multiplexer when a single variable MEV is permitted. $f(A,B,C,D) = \sum m(0,2,3,8,10,11,12,14)$	**08**	(3 :2: 1.7.1)

OR

6.	**a.**	Draw the logic diagram for a 2:4 logic Decoder with an active low enable and active high data output. Construct the truth table and draw the logic symbol for a decoder. Describe the circuit function.	**06**	(2:2: 1.6.1)
	b.	Show that a full adder can be converted to a full subtractor.	**06**	(3 :2: 1.7.1)
	c.	Design a 4-bit comparator that propagates its secondary signal from left to right a. Sketch a block diagram with input and outputs. b. Construct a truth table c. Write the minterm equation for the outputs. d. Simplify output equation and draw the diagram.	**08**	(3 :2: 1.7.1)

MODULE – 4

7.	**a.**	Draw the logic diagram. Construct the excitation table and write the characteristic equation for a) J K Flip-flop b) T flip-flop	**06**	(2 :3: 1.7.1)
	b.	Determine the final output states over time for the following circuit, built from D-type gated latches: 	**06**	(3 :3: 1.7.1)

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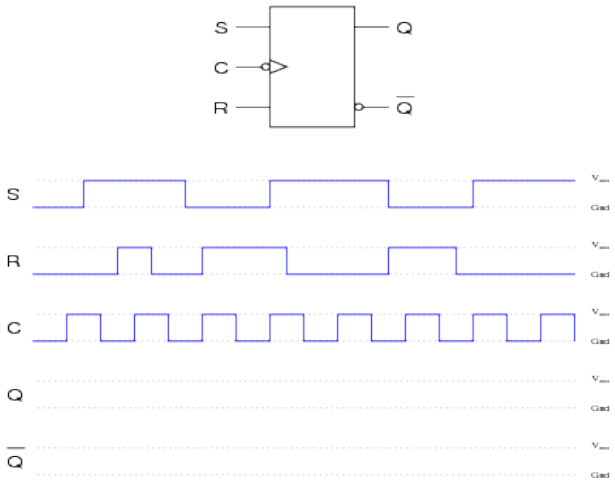
	c.	Design 3-bit synchronous up counter using JK flip flops.	08	(3 :3: 1.7.1)

OR

8.	a.	Sketch the model diagrams for a Mealy and Moore sequential circuit. Describe the difference between Mealy and Moore circuit.	06	(2 :3: 1.6.1)
	b.	Determine the output states for this S-R flip-flop, given the pulse inputs shown:  	06	(3 :3: 1.7.1)
	c.	A 4-bit serial in parallel out shift register is initially set to 1111. The data 1010 is applied to the inputs. Sketch the output waveforms after 3 clock cycles. (Hint: for serial data LSB first)	08	(3 :3: 1.7.1)

MODULE – 5

9.	a.	(i) Declare a register called oscillate. Initialize it to 0 and make it toggle every 30-time units. (ii)Design a clock with time period = 40 and a duty cycle of 25% by using the always and initial statements. The value of clock at time = 0 should be initialized to 0.	06	(2 :4: 1.6.1)
	b.	Write a Verilog dataflow description for 4:1 multiplexer using Conditional operator.	06	(3 :4: 1.7.1)
	c.	Write a Verilog code to detect a pattern 1101(MSB first) using Moore circuit.	08	(3 :4: 1.7.1)

OR

10.	a.	Given below is an initial block with blocking procedural assignments. At what simulation time is each statement executed? What are the intermediate and final values of a, b, c, d?
		initial
		begin
		a = 1'b0;
		b = #10 1'b1;
		c = #5 1'b0;
		d = #20 {a, b, c};
			06	(2 :4: 1.7.1)

	b.	Write a Verilog gate level description for 4-bit ripple carry full adder by instantiating four 1-bit Full adders also describe 1-bit Full adder using gate level description.	06	(3 :4: 1.7.1)
	c.	Write a Verilog code to detect a pattern 10101(MSB first) using Mealey circuit.	08	(3 :4: 1.7.1)

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