Basavarajeswari Group of Institutions

BALLARI INSTITUTE OF TECHNOLOGY & MANAGEMENT

(Autonomous Institute under Visvesvaraya Technological University, Belagavi)

USN											Course Code	2	1	E	C	3	4

Third Semester B.E. Degree Examinations, March/April 2023

ANALOG ELECTRONIC CIRCUITS

Duration: 3 hrs **Max. Marks: 100**

Note: *1. Answer any* **FIVE** *full questions, choosing* **ONE** *full question from each module.*
2. Missing data, if any, may be suitably assumed

Q. No		*Question*	*Marks*	*(RBTL:CO: PI)*
		MODULE – 1		
1.	**a.**	Describe the Characteristics of PN junction with necessary equations	**06**	(1 :1: 1.3.1)
	b.	Explain the Centre-Tapped full wave rectifier and calculate the efficiency for the same	**06**	(2 :1: 1.3.1)
	c.	Explain the working of positive and Negative clamper	**08**	(2 :1: 1.3.1)
		OR		
2.	**a.**	Explain the Construction and operation of JFET and also write the symbols of n-channel and p-channel JFET	**06**	(2 :1: 1.3.1)
	b.	Write a short note on Positive Fixed Voltage Regulator Negative Fixed Voltage Regulator Adjustable Voltage Regulator	**08**	(2 :1: 1.3.1)
	c.	Explain the Construction and operation of BJT with Carrier Flow diagram	**06**	(2 :1: 1.3.1)
		MODULE – 2		
3.	**a.**	Obtain the DC Conditions for Voltage Divider Bias Circuit for a CE-BJT Amplifier and give design constraints along with remark on Stability of Q-Point	**08**	(2 :2: 1.3.1)
	b.	For CE Amplifier circuit VBE is adjusted to yield a DC Collector current of 1mA.Let V_{CC}=15V, Rc=10KΩ and β=150 Find the Voltage Gain. If VBE=0.002 sinωt Volt, Find $V_c(t)$ and $i_B(t)$.	**08**	(3 :2: 2.1.2)
	c.	A BJT having β=100 is biased at DC Collector Current of 1mA.Find the Value of g_m, re and r_π at the bias point. Assume $V_\gamma = \frac{1}{40}V$	**04**	(3 :2: 2.1.2)
		OR		
4.	**a.**	Draw the small signal equivalent circuit model for MOSFET and obtain the expression for voltage gain	**06**	(2 :2: 1.3.1)
	b.	Design a circuit to fix V_G and bias using R_s and Voltage divider arrangement to establish DC Drain current of 0. 5mA.The MOSFET is specified to have V_t=1V, $K'_n\frac{W}{L} = \frac{1mA}{V^2}$ use V_{DD}=15V.	**08**	(3 :2: 1.7.1)
	c.	Mention the relation between r_π and r_e	**06**	(2 :2: 1.3.1)
		MODULE – 3		

Note: (**RBTL - Revised Bloom's Taxonomy Level: CO - Course Outcome: PI - Performance Indicator)**

5.	**a.**	Obtain the expression for R_{in}, R_o $A_{v\ for}$ a Common Drain amplifier or source amplifier using suitable AC Equivalent circuit.	**8**	(2 :3: 1.3.1)
	b.	Explain the high frequency response of CS Amplifier using MOSFET and derive its upper cut-off Frequency.	**6**	(2 :3: 1.3.1)
	c.	With Mathematical equations, explain the different internal capacitances in the MOSFET	**6**	(2 :3: 1.3.1)
		OR		
6.	**a.**	Obtain the low frequency response of CS amplifier.	**10**	(2 :3: 1.3.1)
	b.	Write a Short note on 1. Current Source 2. Current Mirror	**10**	(1:3: 1.3.1)
		MODULE – 4		
7.	**a.**	Explain the four basic Feedback topologies	**10**	(2 :4: 1.3.1)
	b.	With neat block diagram explain the working of a voltage series feedback amplifier obtain expressions for gain, input resistance and output resistance with feedback.	**10**	(3 :4: 1.3.1)
		OR		
8.	**a.**	What is output stage and discuss the classification of output stages based on the Collector current?	**10**	(2 :4: 1.3.1)
	b.	Explain the working of Class output stage amplifier and also prove that power conversion efficiency 25%.	**10**	(3 :4: 1.3.1)
		MODULE – 5		
9.	**a.**	Explain the Working of Instrumentation amplifier using transducer bridge and derive the expression of output voltage	**10**	(3 :5: 1.3.1)
	b.	Explain the operation of Successive approximation DAC and mention its advantages	**10**	(2 :5: 1.3.1)
		OR		
10.	**a.**	Explain the working of a first order active filter with circuit and frequency response	**10**	(2 :5: 1.3.1)
	b.	Design an Astable Multivibrator using 555 timer with 1. f_0=1KHz and Duty Cycle=25% 2. f_0=2KHz and Duty Cycle=50% 3. f_0=2KHz and Duty Cycle=75%	**10**	(3 :5: 2.3.1)

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