Basavarajeswari Group of Institutions

BALLARI INSTITUTE OF TECHNOLOGY & MANAGEMENT

(Autonomous Institute under Visvesvaraya Technological University, Belagavi)

USN										Course Code	2	2	E	E	3	2

Third Semester B.E. Degree Examinations, March/April 2024

DIGITAL ELECTRONICS

Duration: 3 hrs **Max. Marks: 100**

Note: 1. Answer any* FIVE *full questions choosing ONE full Question from each Module.
2. Missing data, if any, may be suitably assumed

Q. No		*Question*	*Marks*	*(RBTL:CO:PI)*
		Module-1		
1.	**a.**	Define combinational logic. Explain the steps involved in designing the combinational logic circuit with block diagram.	**10**	(2:1: 1.4.1)
	b.	Place the following expressions in the Canonical/Standard form: (i) $f(x,y,z) = (xy+z')(y+xz')$ (ii) $f(a,b,c,d) = (a+b)(b+c')$	**10**	(3 :1: 2.1.2)
		(OR)		
2.	**a.**	Using Karnaugh maps, determine all the prime implicants for each of the following incomplete Boolean functions. In each case, indicate which is essential. (i) $f(w,x,y,z) = \sum m(0,2,5,7,8,10,13,15) + dc(1,4,11,14)$ (ii) $f(w,x,y,z) = \sum m(1,3,5,7,8,10,12,13,14) + dc(4,6,15)$	**10**	(3 :1: 2.1.2)
	b.	Explain the following terms with examples (i) Literal (ii) SOP and POS term (iii) Min term and Max term (iv) Canonical SOP (v) Canonical POS	**10**	(3 :1: 2.1.2)
		Module-2		
3.	**a.**	Design full adder. Construct a truth table and simplify each output equation using Kmap.	**08**	(3 :2: 2.4.1)
	b.	Design 1 bit comparator using logic gates.	**04**	(3 :2: 2.4.1)
	c.	Implement the following function f(a,b,c,d)=Σm(1,5,6,7,9,10,15) using 4:1 using MUX with a,b as select lines.	**08**	(2 :1: 1.4.1)
		(OR)		
4.	**a.**	Design 4:2 line priority encoder.	**08**	(3 :2: 2.4.1)
	b.	Implement the following functions using 74138IC and logic gates. F1(a,b,c)=Σm(0,2,4) F2(a,b,c)=Σm(1,2,4,5,7)	**04**	(3 :2: 2.1.2)
	c.	Design 4 bit carry look Ahead adder and explain how propagation delay is eliminated.	**08**	(3 :2: 2.4.1)
		Module-3		
5.	**a.**	Distinguish between sequential circuits and combinational circuits.	**04**	(2 :3: 1.4.1)
	b.	Explain the application of SR latch as switch debouncer.	**08**	(2 :3: 1.4.1)
	c.	Explain master-slave JK flip flop with logic diagram, symbol, truth table and timing diagram.	**08**	(2 :3: 1.4.1)
		(OR)		

Note: (RBTL - Revised Bloom's Taxonomy Level: CO - Course Outcome: PI– Performance Indicator)

6.	**a.**	Explain the working of SR Flip-Flop and also represent SR flip flop using NAND-NAND logic diagram.	**08**	(2 :3: 1.4.1)
	b.	With the help of neat logic diagram and waveforms, explain positive edge triggered D flip flop.	**08**	(2 :3: 1.4.1)
	c.	Obtain characteristic equations for D and T flip-flop.	**04**	(2 :3: 1.4.1)

Module-4

7.	**a.**	Explain the working of SISO shift register for left shift mode.	**08**	(2 :4: 1.4.1)
	b.	Design BCD asynchronous counter using JK flip-flop.	**08**	(3 :4: 1.4.1)
	c.	Explain the working of PIPO shift register.	**04**	(2 :4: 2.1.2)

(OR)

8.	**a.**	Explain the working of asynchronous up/down counter.	**08**	(2 :4: 1.4.1)
	b.	Design MOD 6 counter using positive edge triggered JK flip-flop for $0 \rightarrow 2 \rightarrow 3 \rightarrow 6 \rightarrow 5 \rightarrow 1$.	**08**	(3 :4: 2.1.2)
	c.	Differentiate synchronous counter and asynchronous counter.	**04**	(2 :4:1.4.1)

Module-5

9.	**a.**	Explain Moore and Mealy models with relevant block diagrams	**08**	(2 :5: 1.4.1)
	b.	Construct state table and state diagram for the following sequential circuit shown in Fig. 9(b).	**12**	(3 :5: 2.1.2)

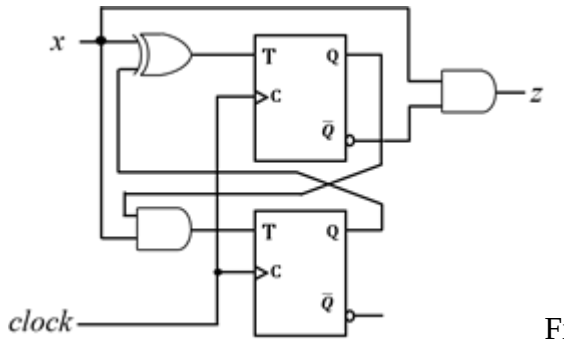

Fig. 9(b)

(OR)

10	**a.**	Explain state machine notations with examples and relevant diagrams.	**08**	(2 :5: 1.4.1)
	b.	Construct state table and state diagram for the following sequential circuit shown in Fig. 10(b).	**12**	(3 :5: 2.1.2)

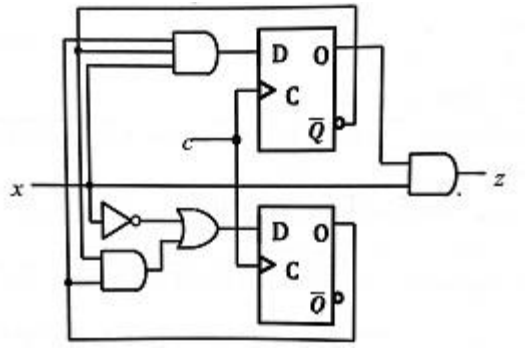

Fig. 10(b)

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