USN | | | | | | | | | | Course Code | 2 | 2 | E | C | 3 | 6 | 1

Third Semester B.E. Degree Examinations, March/April 2024
COMPUTER ORGANIZATION AND ARCHITECTURE

Duration: 3 hrs   **Max. Marks: 100**

*Note: 1. Answer any **FIVE** full questions, choosing **ONE** full question from each module.*
2. Missing data, if any, may be suitably assumed

Q. No		*Question*	*Marks*	*(RBTL:CO:PI)*
		Module-1		
1.	**a.**	**Design** 32-bit address line memory space. Locate **lower and upper** order addresses along with memory location addresses with neat diagram.	**04**	(2 :1 : 1.7.1)
	b.	Explain the basic performance equation for a computer system along with effect of parameters. Also write importance of processor clock.	**06**	(1 :1 : 1.6.1)
	c.	With the help of neat block diagram, explain basic functional units of a computer system.	**10**	(1 :1 : 1.6.1)
		(OR)		
2.	**a.**	**Represent** the decimal values **10 and -12**, as signed, **5-bit** numbers in the following binary formats. (i) Sign-and-magnitude (ii) 1's-complement (iii) 2's-complement Also perform **addition of numbers using 2's complement method**.	**06**	(2 :1 : 1.7.1)
	b.	**Define** (i) Timing signal (ii) Big-endian and Little-endian (iii) Data (iv) Stored program (v) Bus and Single bus (vi) Multitasking	**06**	(1 :1 : 1.6.1)
	c.	Explain OS routine sharing of the processor with a neat timeline diagram.	**08**	(1 :1 : 1.6.1)
		Module-2		
3.	**a.**	Write an ALP to multiply two decimal numbers: 10 and 5 using (i) Register (ii) Indirect addressing modes Write EA in each case.	**06**	(2 :2 : 1.7.1)
	b.	Write an instruction to load 300 in memory location 1000 using any **addressing mode and using assembler directive**. Explain the difference.	**06**	(2 :2 : 1.7.1)
	c.	Stack operation is FIFO. Justify using PUSH and POP Code.	**08**	(1 :2 : 1.6.1)
		(OR)		
4.	**a.**	Perform following operations and find the results if R_0 = 1101_1001_0010_0110, Carry bit = 1 (i) LshiftL #3, R_0 (ii) AshiftR #3, R_0 (iii) RotateLC #3, R_0	**06**	(2 :2 : 1.7.1)
	b.	How basic I/O operations are performed using program controlled I/O applying concept of **separate INSTATUS and OUTSTATUS register.**	**06**	(2 :2 : 1.6.1)
	c.	Define & Explain Subroutine, subroutine nesting and the processor stack.	**08**	(1 :2 : 1.6.1)
		Module-3		
5.	**a.**	Explain vectored interrupts and interrupt nesting methods of handling multiple devices while using interrupts.	**06**	(1 :3 : 1.6.1)
	b.	Explain following two methods of accessing I/O devices: (i) Memory mapped I/O (ii)I/O mapped I/O(Isolated I/O).	**06**	(1 :3 : 1.6.1)

Note: (RBTL - Revised Bloom's Taxonomy Level: CO - Course Outcome: PI– Performance Indicator)

	c.	Write detailed explanation of DMA.	**08**	(1 :3 : 1.6.1)

<div align="center">(OR)</div>

6.	a.	Explain the transfer of control through the use of interrupts.	**06**	(1 :3 : 1.6.1)
	b.	Differentiate between subroutine and ISR	**06**	(1 :3 : 1.6.1)
	c.	Explain Interrupt Hardware and enabling & disabling of interrupts.	**08**	(1 :3 : 1.6.1)

<div align="center"><u>Module-4</u></div>

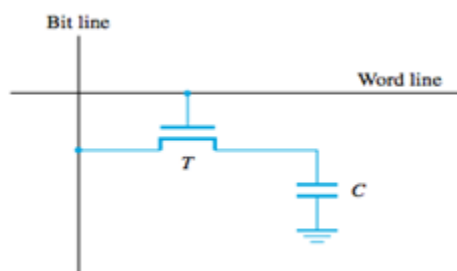|				
7.	a.	Consider the dynamic memory cell of Fig. Q7 (a). Assume that C = 50 femtofarads (10^{-15} F) and that leakage current through the transistor is about 0.5 Pico amperes (10^{-12} A). The voltage across the capacitor when it is fully charged is 2.5 V. The cell must be refreshed before this voltage drops below 1.2 V. Estimate the minimum refresh rate.	**06**	(2 :4 : 1.7.1)

<div align="center">Fig. Q7(a)</div>

	b.	Write a short note on cache Memory.	**06**	(1 :4 : 1.6.1)
	c.	Enlighten the Internal organization of a 2Mx 8 dynamic memory chip. How is fast page mode achieved?	**08**	(1 :4 : 1.6.1)

<div align="center">(OR)</div>

8.	a.	A disk unit has 24 recording surfaces. It has a total of 15000 cylinders. There is an average of 600 sectors per track. Each sector contains 512 bytes of data. (i) What is the maximum number of bytes that can be stored in this unit? (ii) What is the data transfer rate in bytes/sec at a rotational speed of 7200 RPM?	**06**	(2 :4 : 1.7.1)
	b.	Write a short note on static memories	**06**	(1 :4 : 1.6.1)
	c.	Explain about organization of one surface of the magnetic disk with the help of diagram.	**08**	(1 :4 : 1.6.1)

<div align="center"><u>Module-5</u></div>

9.	a.	Show the circuit implementation of Z_{in} generation and end control signal generation using hard wired control.	**06**	(1 :5 : 1.6.1)
	b.	Explain input and output gating for the registers along with single bus organization of the data path inside a processor with the help of appropriate diagrams.	**06**	(1 :5 : 1.6.1)
	c.	Write the control sequence for the following instruction using three bus organization along with explanation and appropriate diagram: MUL R0, R1, R6	**08**	(1 :5 : 1.6.1)

<div align="center">(OR)</div>

10	a.	Explain three-bus organization of the data path with the help of appropriate diagrams.	**06**	(1 :5 : 1.6.1)
	b.	Write the control sequence for the following instructions and explain: ADD (R1), R4.	**06**	(1 :5 : 1.6.1)
	c.	Differentiate between hardwired control and micro programmed control.	**08**	(1 :5 : 1.6.1)

<div align="center">** ** **</div>

Note: (RBTL - Revised Bloom's Taxonomy Level: CO - Course Outcome: PI– Performance Indicator)